■ Tentative Specification
☐ Preliminary Specification
☐ Approval Specification

MODEL NO.: G057VCE
SUFFIX: TH1

Customer:

APPROVED BY **SIGNATURE**

Name / Title _____ _____
Note

Please return 1 copy for your confirmation with your signature and comments.

Approved By	Checked By	Prepared By

CONTENTS

REVISION HISTORY

Version	Date	Page	Description
Ver 0.0	12 Oct 2021	All	Tentative Specification was first issued.

1. GENERAL DESCRIPTION

1.1 OVERVIEW

G057VCE-TH1is a 5.7” TFT Liquid Crystal Display IAV module with LED Backlight units and 40 pins 1ch-TTL interface. This module supports 640 x 480 VGA mode and can display 262k colors.

The PSWG is to establish a set of displays with standard mechanical dimensions and select electrical interface requirements for an industry standard 5.7” VGA LCD panel and the LED driving device for Backlight is built in PCBA.

1.2 FEATURE

- VGA (640 x 480 pixels) resolution
- DE (Data Enable) mode and DE+SYNC mode selection
- TTL Interface
- PSWG (Panel Standardization Working Group)
- Wide operating temperature.
- Reversible scan direction
- RoHS compliance

1.3 APPLICATION

-TFT LCD Monitor

- Factory Application
- Amusement

1.4 GENERAL SPECIFICATI0NS

Item	Specification	Unit	Note
Active Area	115.2 (H) x 86.4 (V) (5.7” diagonal)	mm	(1)
Driver Element	a-Si TFT active matrix	-	-
Pixel Number	640 x R.G.B x 480	pixel	-
Pixel Pitch	0.18(H) x 0.18(W)	mm	-
Pixel Arrangement	RGB vertical Stripe	-	-
Display Colors	262K	color	-
Display Mode	Normally Black	-	-
Surface Treatment	Hard Coating (3H), Anti-Glare	-	-
Module Power Consumption	TBD(PanelTBD+BL 2.3W)	W	Typ.

1.5 MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal(H)	143.5	144	144.5	mm	(1)
	Vertical(V)	104.1	104.6	105.1	mm	
	Depth(D)	11.8	12.3	12.8	mm	
Bezel Area	Horizontal	117.6	118.2	118.4	mm	-
	Vertical	88.8	89.4	89.6	mm	
Active Area	Horizontal	-	115.2	-	mm	
	Vertical	-	86.4	-	mm	
Weight		-	(TBD)		g	

Note (1)Please refer to the attached drawings for more information of front and back outline dimensions.

2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Operating Ambient Temperature	T_{OP}	-30	+85	°C	(1)(2)
Storage Temperature	T_{ST}	-40	+85	°C	

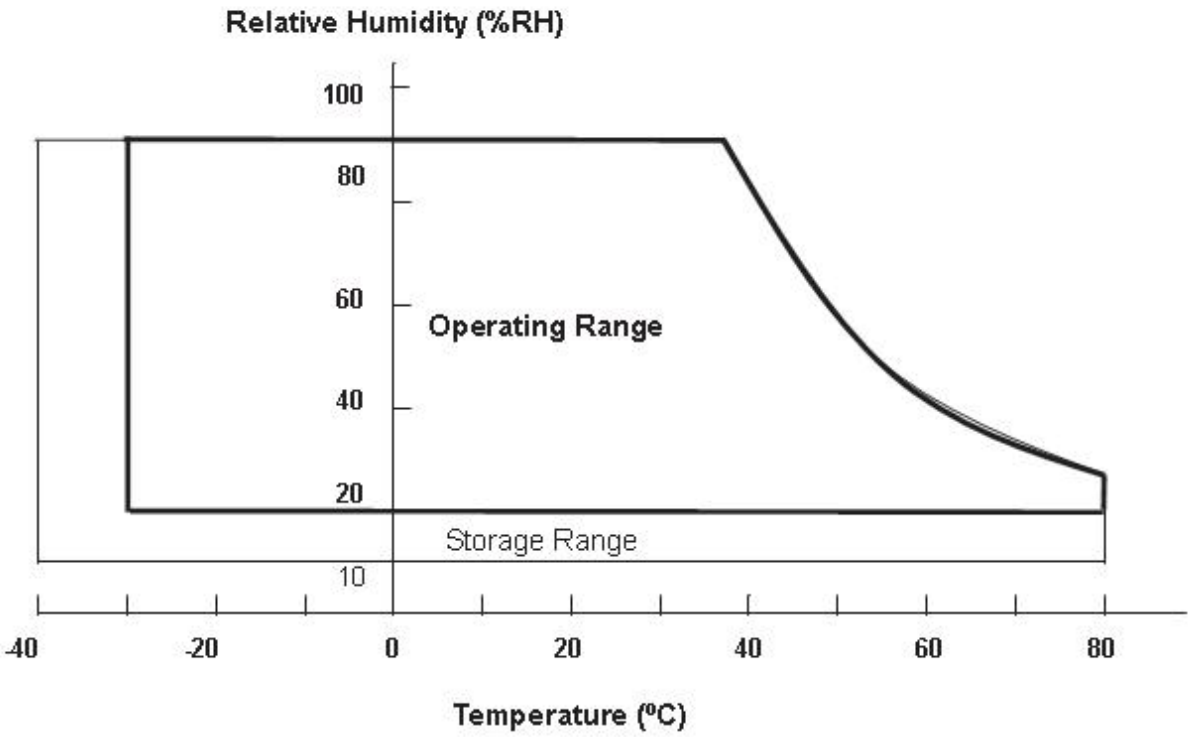
Note (1)

(a) 90 %RH Max.

(b) Wet-bulb temperature should be 39 ºC Max.

(c) No condensation.

Note (2) Panel surface temperature should be 0°C min. and 65°C max under Vcc=5.0V, fr =60Hz, typical LED string current, 25°C ambient temperature, and no humidity control . Any condition of ambient operating temperature ,the surface of active area should be keeping not higher than 85°C.



2.2 ELECTRICAL ABSOLUTE RATINGS

2.2.1 TFT LCD MODULE

Item	Symbol			Unit	Note
		Min.	Max.		
Power Supply Voltage	VCC	-0.3	4	V	(1)
Logic Input Voltage	VIN	-0.3	4	V	

2.2.2 BACKLIGHT UNIT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Converter Voltage	V_i	-0.3	18	V	(1) , (2)
Enable Voltage	EN	---	5.5	V	
Backlight Adjust	Dimming	---	5.5	V	

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

Note (2) Specified values are for LED (Refer to 3.2 for further information).

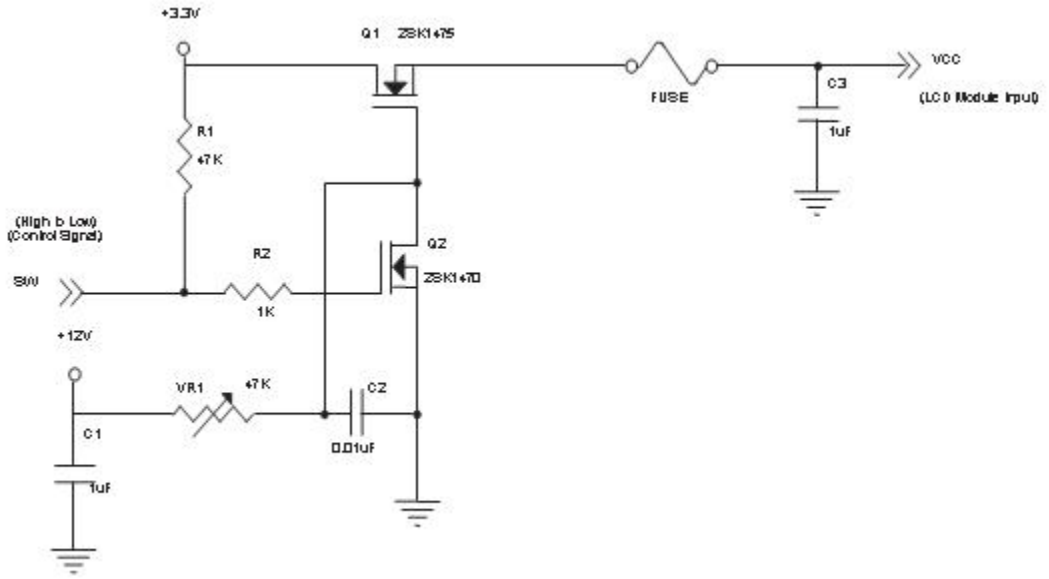
3. ELECTRICAL CHARACTERISTICS

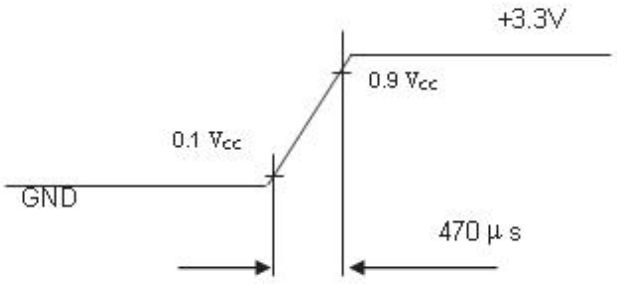
3.1 TFT LCD MODULE

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		V_{CC}	3.0	3.3	3.6	V	-
Ripple Voltage		V_{RP}	-	-	100	mVp-p	
Inrush Current		I_{INRUSH}	-	-	2.0	A	(2)
Power Supply Current	White	Icc	-	TBD	TBD	mA	(3)a
	Black		-	TBD	TBD	mA	(3)b
Power Consumption		P_L	-	TBD	-	W	
Logic High Input Voltage		V_{IH}	$0.7V_{CC}$		V_{CC}	V	
Logic Low Input Voltage		V_{IL}	GND		$0.3V_{CC}$	V	

Note (1)The module should be always operated within above ranges.

Note (2)Measurement Conditions:





Note (3) The specified power supply current is under the conditions at V_{DD} =3.3V, Ta = 25 ± 2 °C, DC Current and f_v = 60 Hz, whereas a power dissipation check pattern below is displayed.

a. White Pattern

Active Area

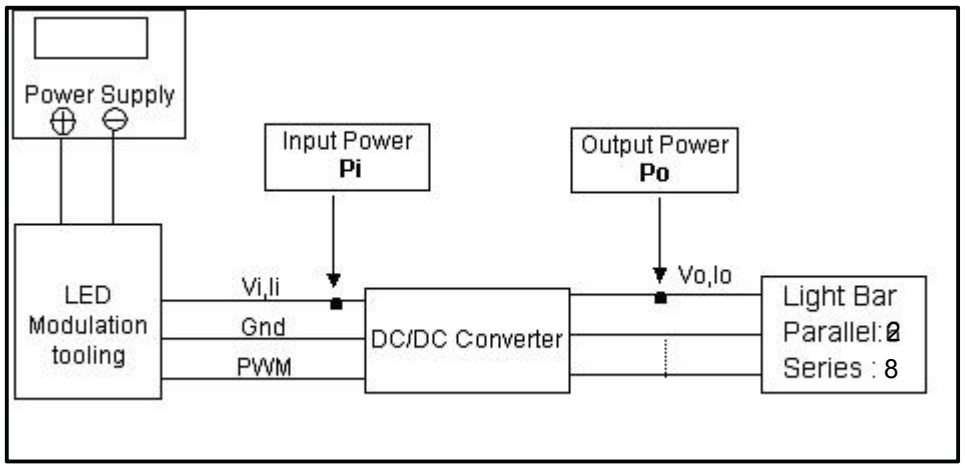
b. Black Pattern

Active Area

3.2 BACKLIGHT UNIT

Parameter		Symbol	Min.	Typ.	Max.	Unit	Note
Converter Input Voltage		V_i	10.8	12.0	13.2	V_{DC}	(Duty 100%)
Converter Input Ripple Voltage		V_{iRP}	-	-	500	mV	
Converter Input Current		I_i	0.16	0.19	0.22	A_{DC}	@ Vi = 12V (Duty 100%)
Converter Inrush Current		I_{Irush}	-	-	3.0	A	@ Vi rising time=10ms (Vi=12V)
Input Power Consumption		P_i	-	2.3		W	(1)
EN Control Level	Backlight on	ENLED (BLON)	2.0	3.3	5.0	V	
	Backlight off		0	-	0.3	V	
PWM Control Level	PWM High Level	Dimming (E_PWM)	2.0	-	5.0	V	
	PWM Low Level		0	-	0.15	V	
PWN Noise Range		VNoise	-	-	0.1	V	
PWM Control Frequency		f_{PWM}	190	200	20k	Hz	(2)
PWM Dimming Control Duty Ratio		-	5	-	100	%	(2), @ 190Hz<f_{PWM}<1kHz
			20	-	100	%	(2), @ 1kHz≤f_{PWM}<20kHz
LED Life Time		L_{LED}	50,000		-	Hrs	(3)

Note (1)LED current is measured by utilizing a high frequency current meter as shown below:



Note (2) The lifetime of LED is estimated data and defined as the time when it continues to operate under the conditions at Ta = 25 ±2 °C and Duty 100% until the brightness becomes ≤ 50% of its original value.

Operating LED at high temperature condition will reduce life time and lead to color shift.

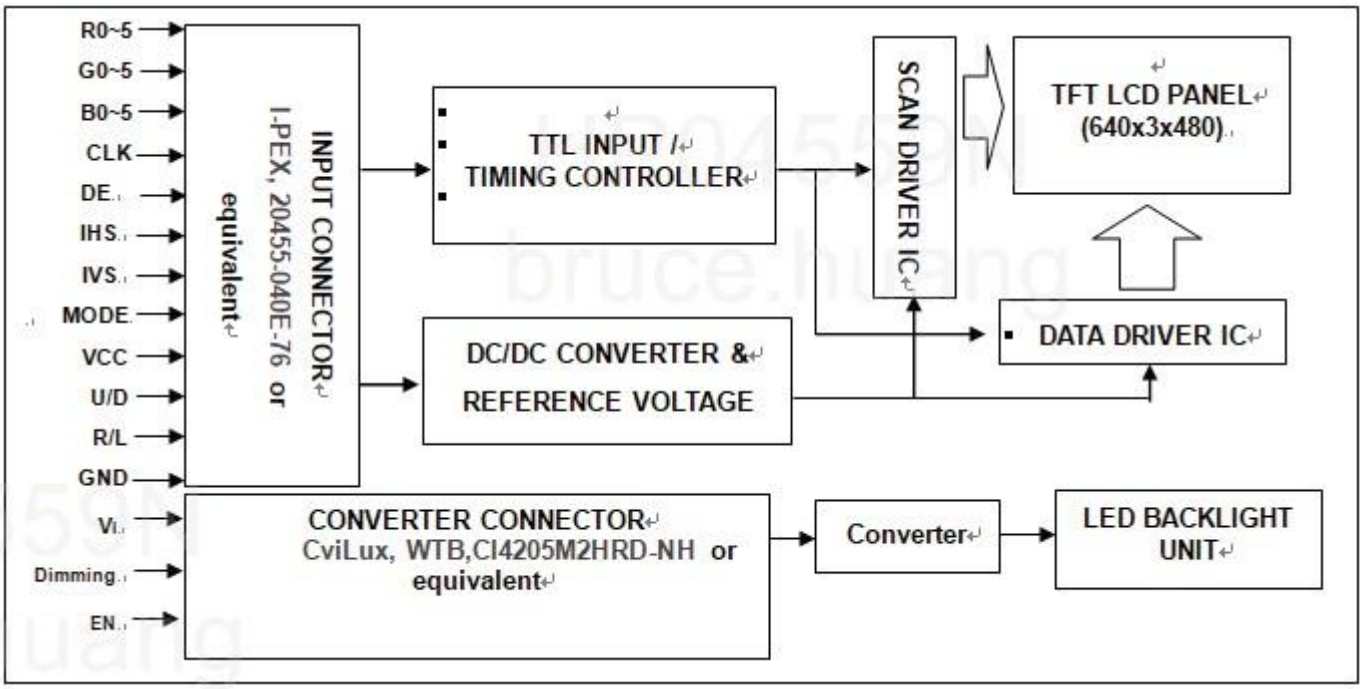
Note (3) At 190 ~1kHz PWM control frequency, duty ratio range is restricted from 5% to 100%.

1K ~20kHz PWM control frequency, duty ratio range is restricted from 20% to 100%.

If PWM control frequency is applied in the range from 1KHz to 20KHZ, The“non-linear”phenomenon on the Backlight Unit may be found. So it is a **suggestion** that PWM control frequency should be **less than 1KHz**.

4. BLOCK DIAGRAM

4.1 TFT LCD MODULE



5. INPUT TERMINAL PIN ASSIGNMENT

5.1 TFT LCD MODULE

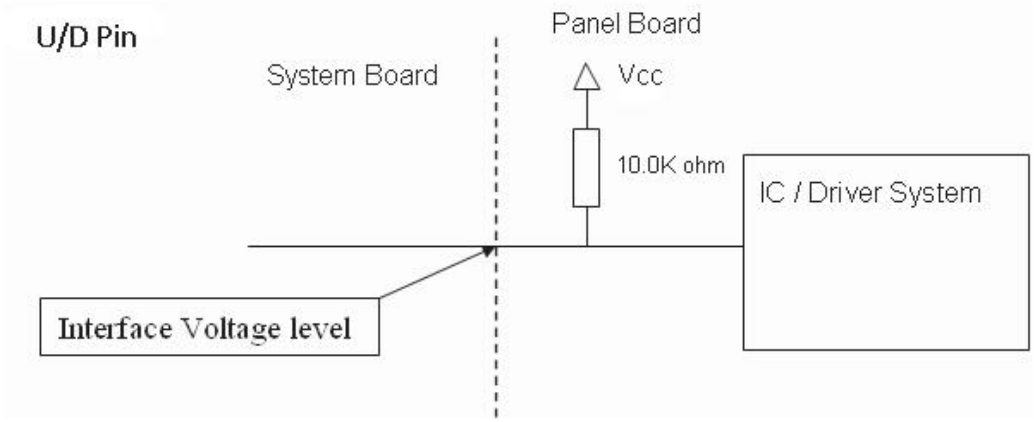
Pin No.	Symbol	Function	Note
1	GND	Ground	
2	CLK	Dot Clock. Latch data at the rising edge.	
3	IHS	Horizontal synchronous signal	
4	IVS	Vertical synchronous signal	
5	GND	Ground	
6	R5	Red data (MSB)	
7	R4	Red data	
8	R3	Red data	
9	R2	Red data	
10	R1	Red data	
11	R0	Red data (LSB)	
12	GND	Ground	
13	G5	Green data (MSB)	
14	G4	Green data	
15	G3	Green data	
16	G2	Green data	
17	G1	Green data	
18	G0	Green data (LSB)	
19	GND	Ground	
20	B5	Blue data (MSB)	Note (3)
21	B4	Blue data	
22	B3	Blue data	
23	B2	Blue data	
24	B1	Blue data	
25	B0	Blue data (LSB)	
26	GND	Ground	
27	DE	Data Enable Signal	
28	NC	No Connection	Note (3)
29	NC	No Connection	Note (3)
30	R/L	Horizontal Reverse Scan Control, Low or NC Normal Mode. High Horizontal Reverse Scan	Note (3)
31	U/D	Vertical Reverse Scan Control, High or NC Normal Mode Low Vertical Reverse Scan	Note (3)
32	NC	No Connection	Note (3) Note (4)
33	NC	No Connection	Note (3) Note (4)
34	NC	No Connection	Note (3) Note (4)
35	MODE	DE / HV mode select. High HV mode. Low or NC DE mode.	Note (3)
36	NC	No Connection	Note (3) Note (4)
37	NC	No Connection	Note (3)
38	VCC	Power supply: +3.3V	
39	VCC	Power supply: +3.3V	
40	VCC	Power supply: +3.3V	

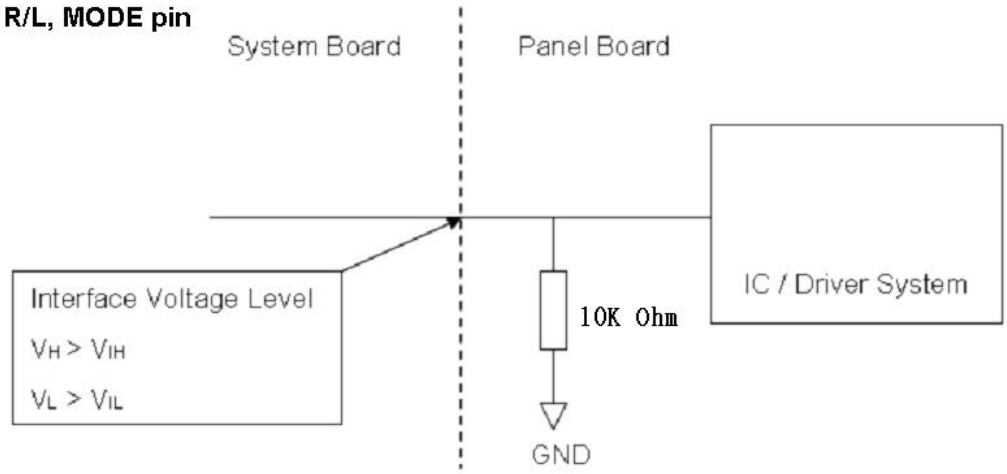
Note (1) Connector Part No.: 20455-040E-76(I-PEX) or equivalent.

Note (2) User's connector Part No.: 20453-040T-03(I-PEX) or equivalent.

Note (3) "Low" stands for 0V. "High" stands for 3.3V. "NC" stands for "No Connection".

Note (4) Pin32, Pin33, Pin34, Pin36 input signals should be set to no connection or ground, this module would operate normally.



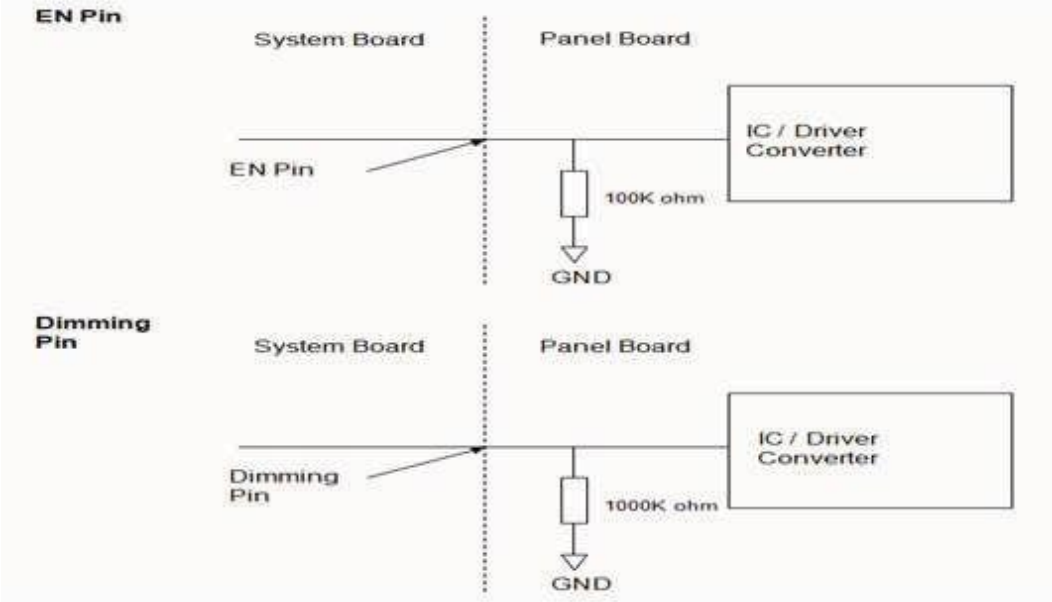


5.2 BACKLIGHT UNIT(Converter connector pin)

Pin	Symbol	Description	Remark
1	NC	Not Connect	
2	Dimming	Backlight Adjust	PWM Dimming (Hi: 3.3V_{DC}, Lo: 0V_{DC})
3	EN	Enable pin	3.3V
4	V_{GND}	Converter ground	Ground
5	V_i	Converter input voltage	12V

Note (1)Connector Part No.: CI4205M2HRD-NH (Cvilux) or equivalent.

Note (2)User's connector Part No.: 9827H-04-N0HF(SWB) or equivalent.



5.3 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 6-bit gray scale data input for the color. The higher the binary input the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																	
		Red						Green						Blue					
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(2)	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red(61)	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(62)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	Green(2)	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
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	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green(61)	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	0
	Green(62)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
	Green(63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Gray Scale Of Blue	Blue(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
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	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(61)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1
	Blue(62)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
	Blue(63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

Note (1)0: Low Level Voltage, 1: High Level Voltage

6. INTERFACE TIMING

6.1 INPUT SIGNAL TIMING SPECIFICATIONS

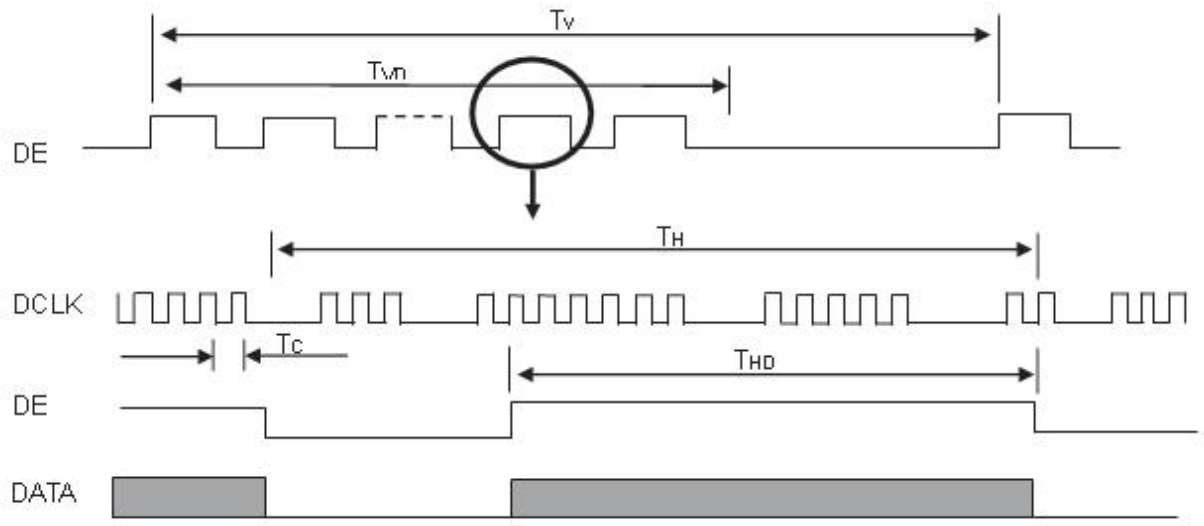
The input signal timing specifications are shown as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
DCLK	Frequency	F_r	20.5	20.7	29.8	MHz	-
	Period	T_c	33.56	48.31	48.78	ns	
	Input cycle to cycle jitter	T_{rcl}	---	---	200	ns	(a)
	Spread spectrum modulation range	F_{clkin_mod}	0.98*Fc	-	1.02*F_c	MHz	(b)
	Spread spectrum modulation frequency	F_{SSM}	-	-	200	KHz	
Vertical Display Term	Frame Rate	F_r	---	60	---	Hz	$Tv=T_{vd}+T_{vb}$
	Total	T_v	488	490	611	T_h	-
	Active Display	T_{vd}	480	480	480	T_h	-
	Blank	T_{vb}	8	10	131	T_h	-
Horizontal Display Term	Total	T_h	700	704	814	T_c	$T_h=T_{hd}+T_{hb}$
	Active Display	T_{hd}	640	640	640	T_c	-
	Blank	T_{hb}	60	64	174	T_c	-

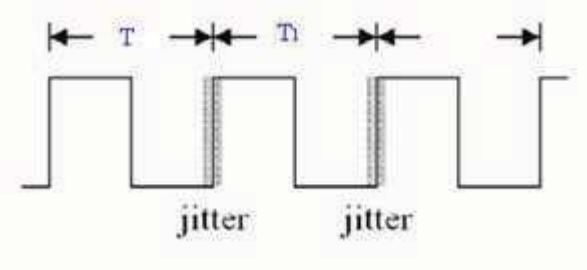
Note (1) Because this module is operated by DE only mode, Hsync and Vsync input signals should be set to low logic level or ground. Otherwise, this module would operate abnormally.

Note (2) The Tv(Tvd+Tvb) must be integer, otherwise, the module would operate abnormally.

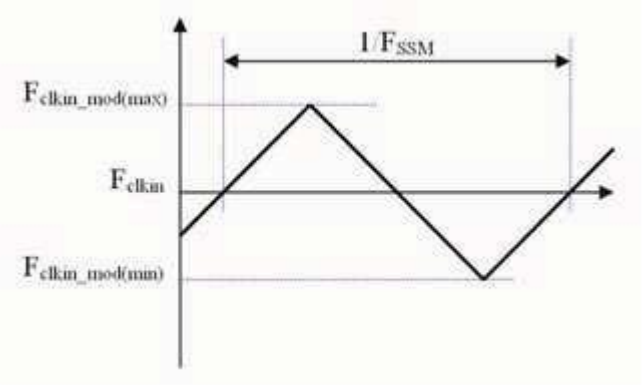
INPUT SIGNAL TIMING DIAGRAM



Note (a) The input clock cycle-to-cycle jitter is defined as below figures. T_{rcl} = I T1 – TI



Note (b) The SSCG (Spread spectrum clock generator) is defined as below figures.



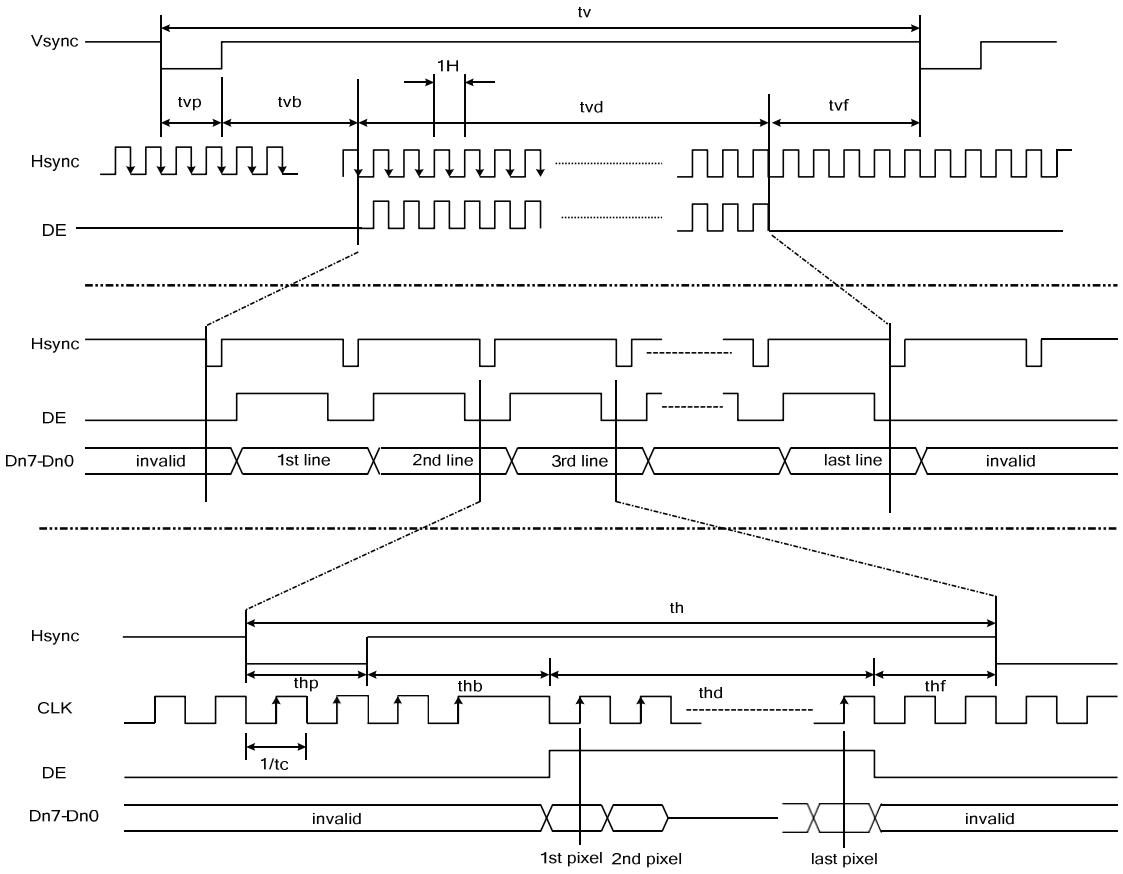
6.2 DE +SYNC MODE INPUT SIGNAL TIMING SPECIFICATIONS

The input signal timing specifications are shown as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
DCLK	Frequency	Tc	20.5	20.7	29.8	MHz	
Vertical Active Display Term	Total	Tv	488	490	611	Th	
	Display	Tvd	-	480	-	Th	
	Front Porch	Tvf	3	5	126	Th	
	Back Porch	Tvb	5	5	5	Th	
	VS Pluse	Tvp	1	2	4	Th	
Horizontal Active Display Term	Total	Th	700	704	814	Tc	
	Display	Thd	-	640	-	Tc	
	Front Porch	Thf	28	32	142	Tc	
	Back Porch	Thb	32	32	32	Tc	
	HS Pluse	Thp	1	2	31	Tc	

Note (1) The Tv(Tvd+Tvb+Tvf+Tvp) must be integer, otherwise, the module would operate abnormally

INPUT SIGNAL TIMING DIAGRAM

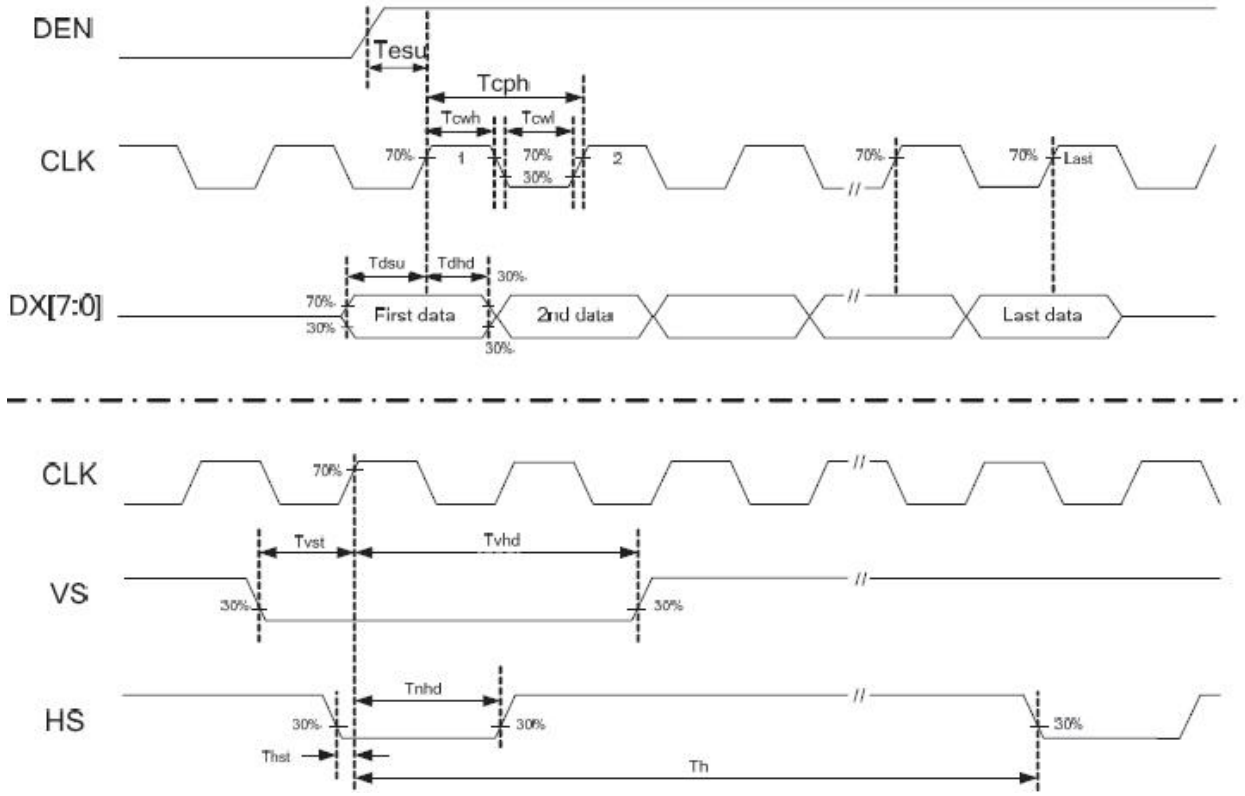


6.3 AC ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Data setup time	Tdsu	10	-	-	ns	Note (1)
Data hold time	Tdhd	10	-	-	ns	Note (1)
DE setup time	Tesu	10	-	-	ns	
HS setup time	Thst	10	-	-	ns	
HS hold time	Thhd	10	-	-	ns	
VS setup time	Tvst	10	-	-	ns	
VS hold time	Tvhd	10	-	-	ns	

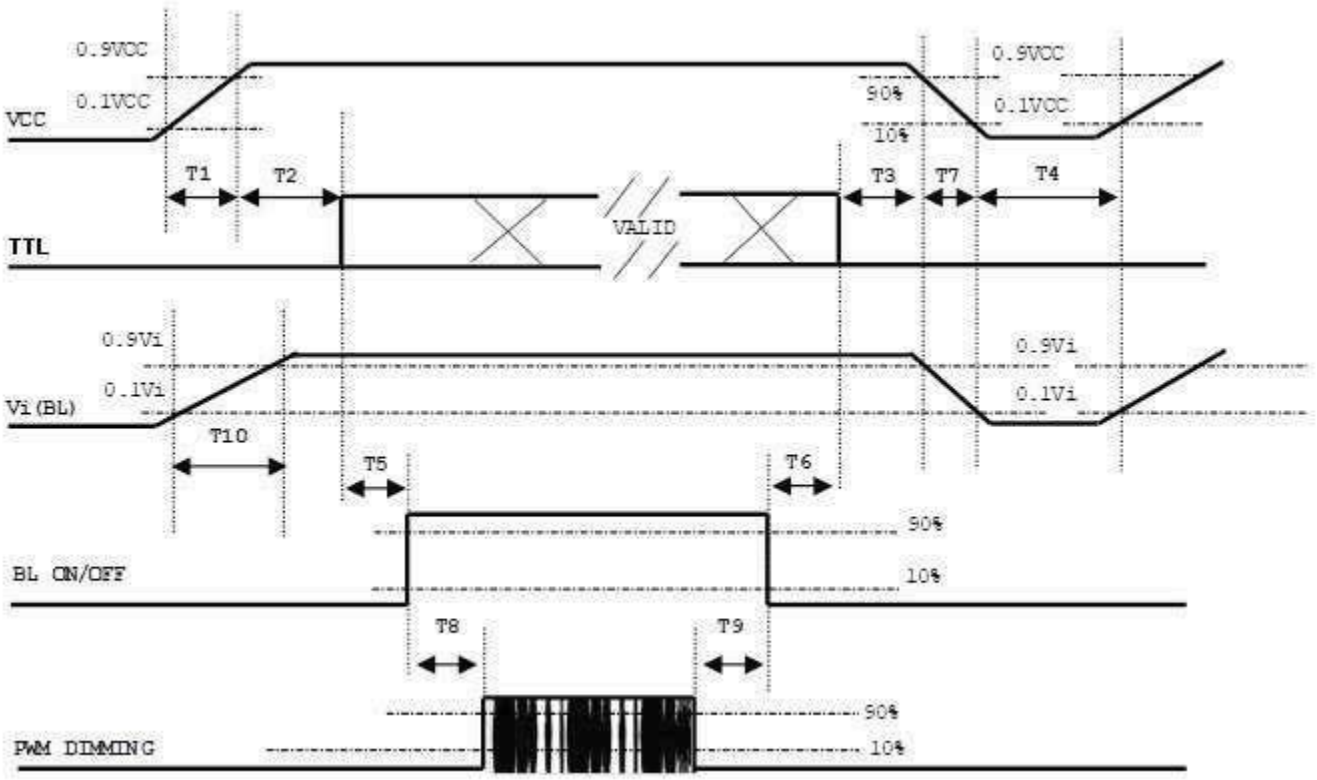
Note (1) CLK latching data at the rising edge.

Clock and Data input waveform



6.4 POWER ON/OFF SEQUENCE

To prevent a latch-up or DC operation of LCD assembly, the power on/off sequence should be as the diagram below.



Parameter	Value			Units
	Min	Typ	Max	
T1	0.5	-	10	ms
T2	0	-	50	ms
T3	0	-	50	ms
T4	500	-	-	ms
T5	450	-	-	ms
T6	200	-	-	ms
T7	10	-	100	ms
T8	10	-	-	ms
T9	10	-	-	ms
T10	20	-	50	ms

Note(1) The supply voltage of the external system for the module input should be the same as the definition of Vcc.

Note(2) When the backlight turns on before the LCD operation of the LCD turns off, the display may momentarily become abnormal screen.

Note(3) In case of VCC = off level, please keep the level of input signals on the low or keep a high impedance.

Note(4) T4 should be measured after the module has been fully discharged between power off and on period.

Note(5) Interface signal shall not be kept at high impedance when the power is on.

Note(6) INX won't take any responsibility for the products which are damaged by the customers not following the Power Sequence.

Note(7) There might be slight electronic noise when LCD is turned off (even backlight unit is also off). To avoid this symptom, we suggest "Vcc falling timing" to follow "T7 spec

6.5 SCANNING DIRECTION

The following figures show the image see from the front view. The arrow indicates the direction of scan.

Fig.1 Normal Scan

Fig.2 Reverse Scan

Fig.3 Reverse Scan

Fig.4 Reverse Scan

PCBA on the top side

PCBA on the top side

Fig. 1 Normal scan (pin 30,R/L=Low or NC, pin 31,U/D = High or NC)

Fig. 2 Reverse scan (pin 30,R/L=High, pin 31,U/D = High or NC)

Fig. 3 Reverse scan (pin 30,R/L=Low or NC, pin 31,U/D = Low)

Fig. 4 Reverse scan (pin 30,R/L=High, pin 31,U/D = Low)

7. OPTICAL CHARACTERISTICS

7.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	oC
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	According to typical value and tolerance in "ELECTRICAL CHARACTERISTICS"		
Input Signal			
PWM Duty Ratio	D	100	%

7.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown here and all items are measured at the center point of screen unless otherwise noted. The following items should be measured under the test conditions described above and stable conditions shown in Note (5).

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Color Chromaticity	Red	Rx	θX=0°, θY =0° Grayscale Maximum	(0.602)	(0.652)	(0.702)	-	(1), (5)
		Ry		(0.286)	(0.336)	(0.386)		
	Green	Gx		(0.271)	(0.321)	(0.371)		
		Gy		(0.553)	(0.603)	(0.653)		
	Blue	Bx		(0.102)	(0.152)	(0.202)		
		By		(0.000)	(0.050)	(0.100)		
	White	Wx		(0.263)	(0.313)	(0.363)		
		Wy		(0.279)	(0.329)	(0.379)		
Center Luminance of White		LC			(360)	(450)		(4), (5)
Contrast Ratio		CR			(600)	(800)		(2), (5)
Response Time		TR	θX=0°, θY =0°	-	(13)	(18)	-	(3)
		TF		-	(12)	(17)	-	
White Variation		δW	θX=0°, θY =0°	(72)	(80)	-	%	(5), (6)
Viewing Angle	Horizontal	θX+	CR≥10	80	88	-	Deg.	(1), (5)
		θX-		80	88	-		
	Vertical	θY+		80	88	-		
		θY-		80	88	-		

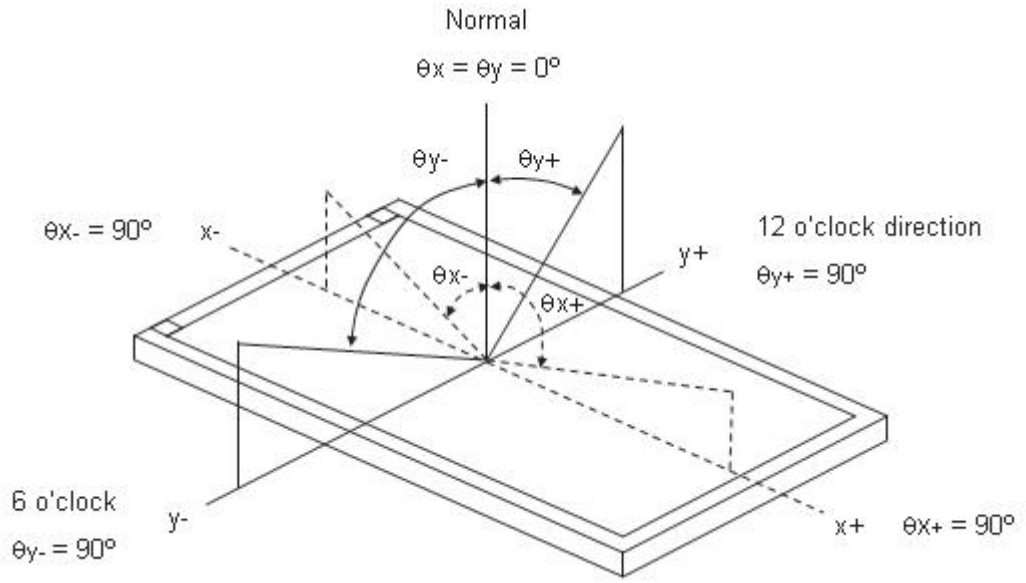
Definition :

Grayscale Maximum : Grayscale 255 (10 bits: grayscale 1023 ; 8 bits : grayscale 255 ; 6 bits: grayscale 63)

White : Luminance of Grayscale Maximum (All R,G,B)

Black : Luminance of grayscale 0 (All R,G,B)

Note (1)Definition of Viewing Angle (θx, θy):

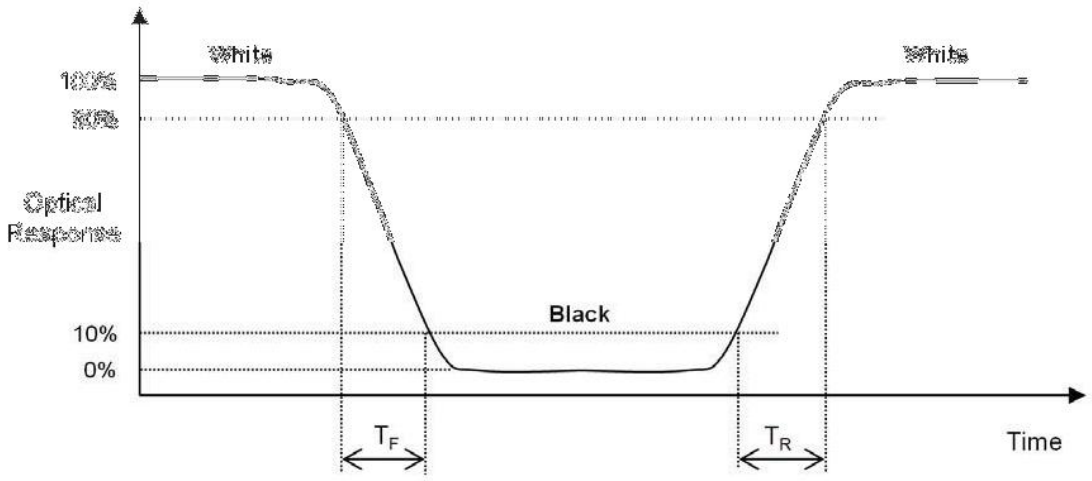


Note (2)Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression at center point.

Contrast Ratio (CR) = White / Black

Note (3)Definition of Response Time (T_R, T_F):

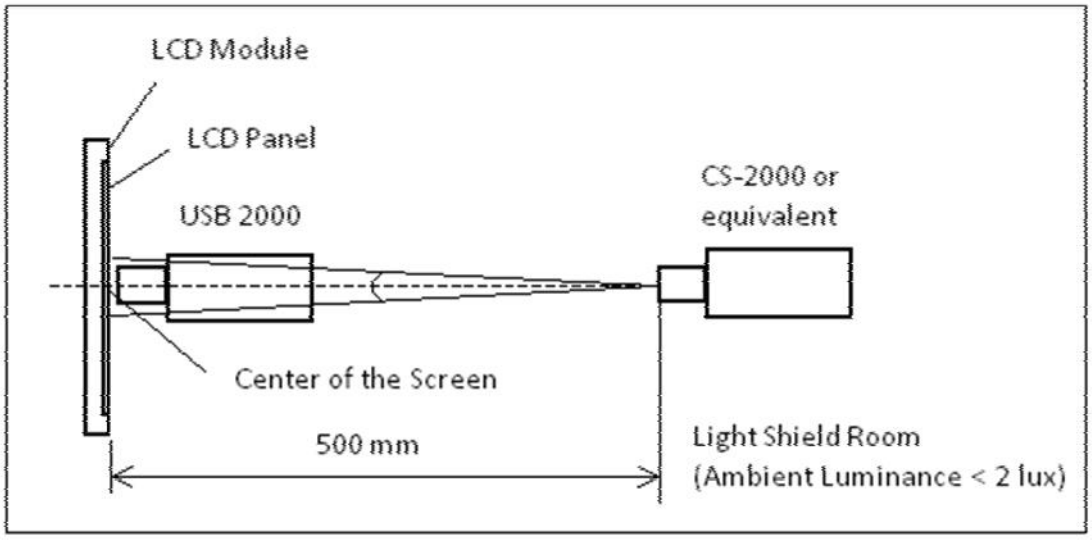


Note (4) Definition of Luminance of White (L_C):

Measure the luminance of White at center point.

Note (5) Measurement Setup:

The LCD module should be stabilized at given temperature to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 40 minutes in a windless room. The measurement placement of module should be in accordance with module drawing.

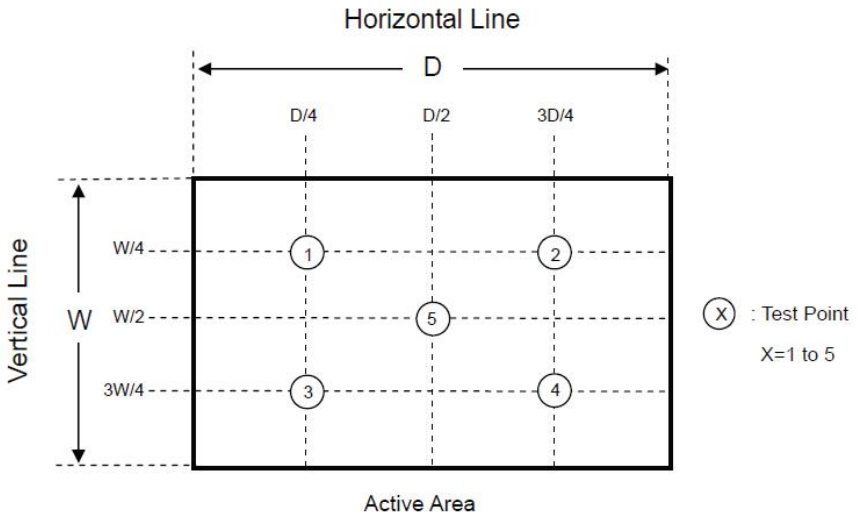


Note (6) Definition of White Variation (δW):

Measure the luminance of White at 5 points.

Luminance of White : L(X) , where X is from 1 to 5.

$$\delta W = \frac{\text{Minimum [L(1) to L(5)]}}{\text{Maximum [L(1) to L(5)]}} \times 100\%$$



8. RELIABILITY TEST CRITERIA

Test Item	Test Condition	Note
High Temperature Storage Test	85℃, 240 hours	(1),(2) (4),(5)
Low Temperature Storage Test	-40℃, 240 hours	
Thermal Shock Storage Test	-30℃, 0.5 hour→→70℃, 0.5 hour; 100cycles, 1 hour/cycle)	
High Temperature Operation Test	85℃, 240 hours	
Low Temperature Operation Test	-30℃, 240 hours	
High Temperature & High Humidity Operation Test	60℃, RH 90%, 240 hours	
ESD Test (Operation)	150pF, 330Ω, 1 sec/cycle Condition 1 : panel contact, ±8 KV Condition 2 : panel non-contact ±15 KV	(1), (4)
Shock (Non-Operating)	50G, 11ms, half sine wave, 1 time for ± X, ± Y, ± Z direction	(2), (3)
Vibration (Non-Operating)	1.5G, 10 ~ 300 Hz sine wave, 10 min/cycle, 3 cycles each X, Y, Z direction	

Note (1)There should be no condensation on the surface of panel during test ,

Note (2) Temperature of panel display surface area should be 85ºC Max.

Note (3) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.

Note (4) In the standard conditions, there is no function failure issue occurred. All the cosmetic specification is judged before reliability test.

Note (5) Before cosmetic and function test, the product must have enough recovery time, at least 24 hours at room temperature.

9. PACKAGING

9.1 PACKING SPECIFICATIONS

(1) 60pcs LCD modules / 1 Box

(2) Box dimensions: 500 (L) X 400 (W) X 330 (H) mm

(3) Weight: approximately 11.65Kg (60 modules per box)

9.2 PACKING METHOD

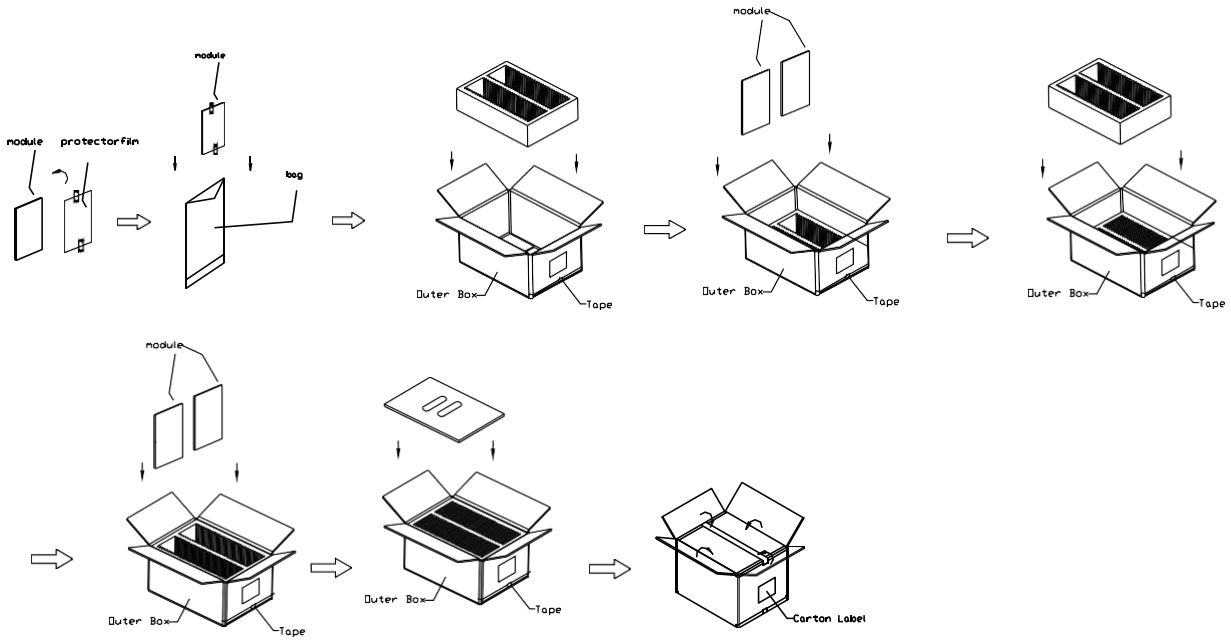


Figure. 9-1 Packing

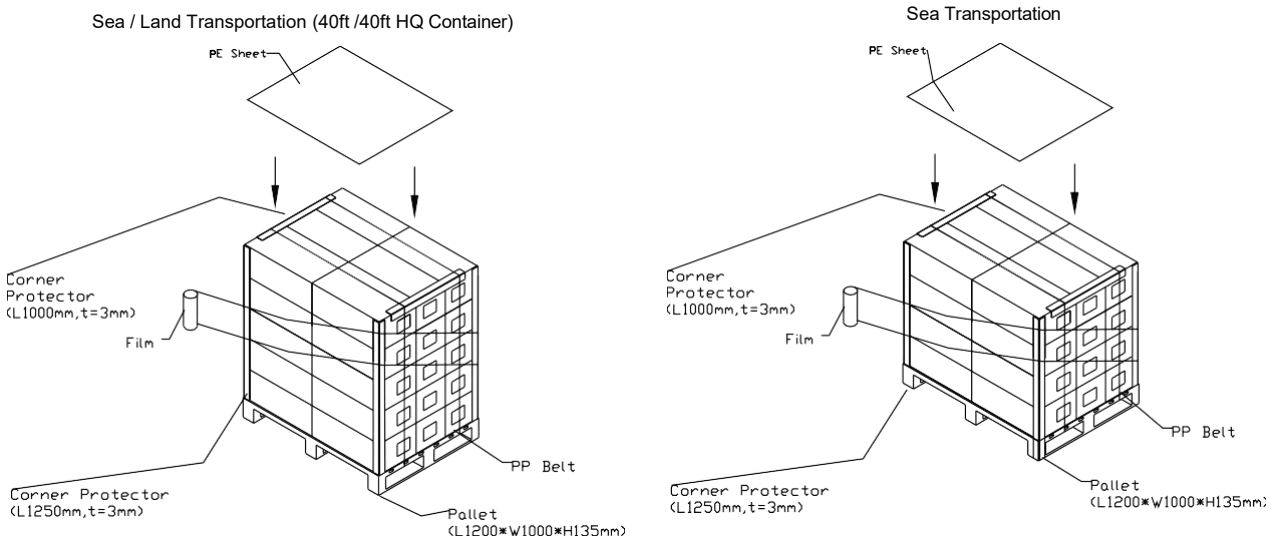


Figure. 9-2 Packing

9.3 UN-PACKING METHOD

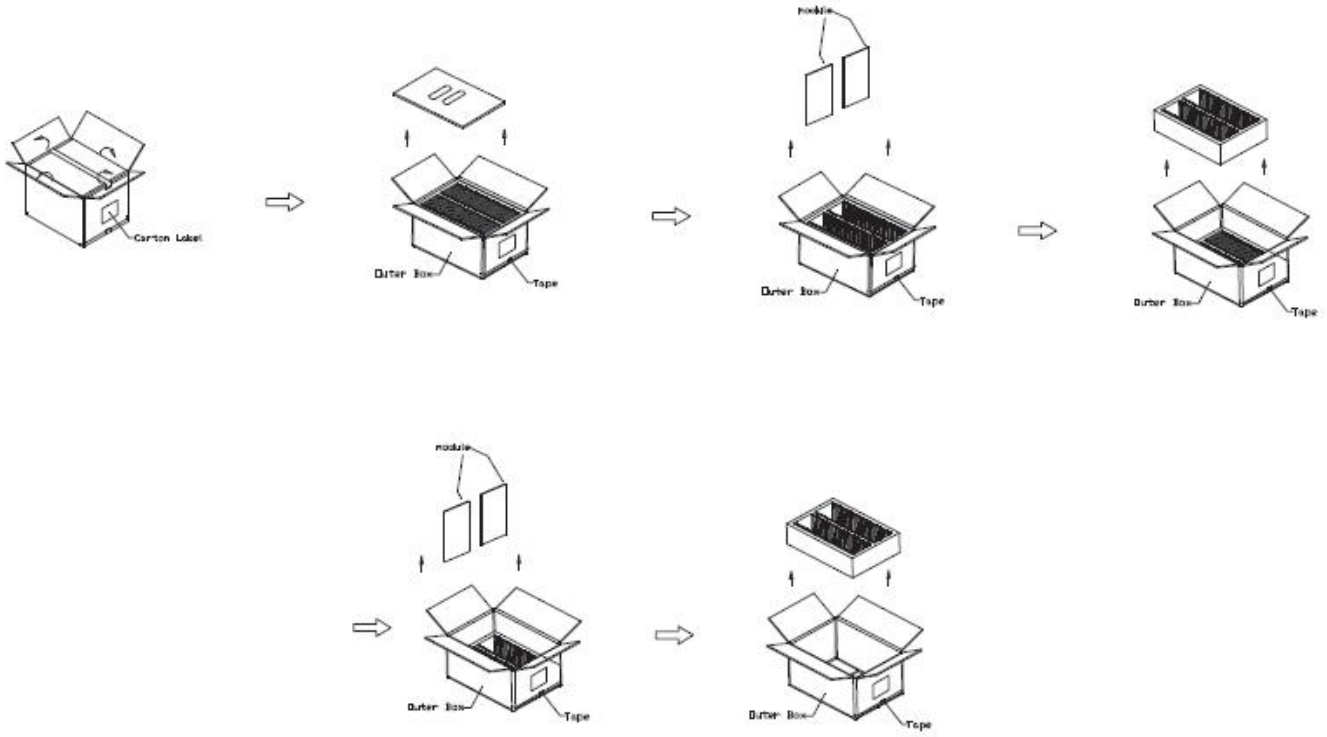
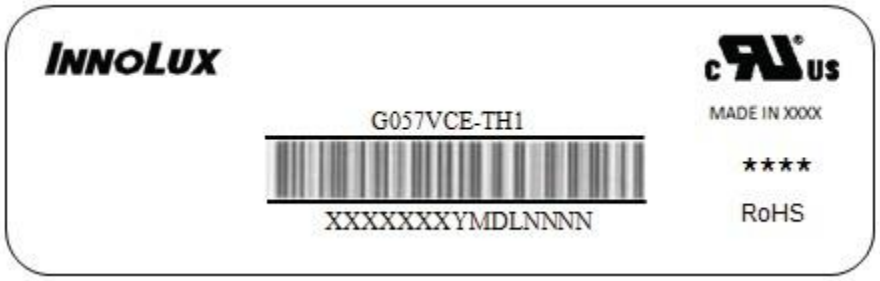


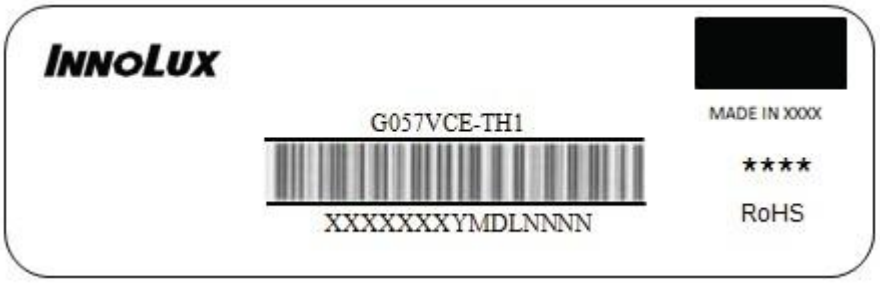
Figure. 9-3 Un-packing method

10. DEFINITION OF LABELS

10.1 INX MODULE LABEL

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



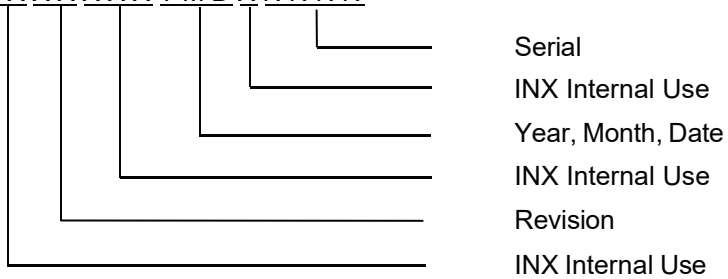


Note (1) Safety Compliance(UL logo) will open after C1 version.

(a) Model Name: G057VCE-TH1

(b) ****: Factory ID

(c) Serial ID: X X X X X X Y M D X N N N N



Serial ID includes the information as below:

(a) Manufactured Date: Year: 1~9, for 2021~2029
Month: 1~9, A~C, for Jan. ~ Dec.
Day: 1~9, A~Y, for 1st to 31st, exclude I , O and U

(b) Revision Code: cover all the change

(c) Serial No.: Manufacturing sequence of product

11. PRECAUTIONS

11.1 ASSEMBLY AND HANDLING PRECAUTIONS

(1) The module should be assembled into the system firmly by using every mounting hole. Be careful not to twist or bend the module.

(2) While assembling or installing modules, it can only be in the clean area. The dust and oil may cause electrical short or damage the polarizer.

(3) Use fingerstalls or soft gloves in order to keep display clean during the incoming inspection and assembly process.

(4) Do not press or scratch the surface harder than a HB pencil lead on the panel because the polarizer is very soft and easily scratched.

(5) If the surface of the polarizer is dirty, please clean it by some absorbent cotton or soft cloth. Do not use Ketone type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanently damage the polarizer due to chemical reaction.

(6) Wipe off water droplets or oil immediately. Staining and discoloration may occur if they left on panel for a long time.

(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contacting with hands, legs or clothes, it must be washed away thoroughly with soap.

(8) Protect the module from static electricity, it may cause damage to the C-MOS Gate Array IC.

(9) Do not disassemble the module.

(10) Do not pull or fold the lamp wire.

(11) Pins of I/F connector should not be touched directly with bare hands.

11.2 STORAGE PRECAUTIONS

(1) When storing for a long time, the following precautions are necessary.

(a) Store them in a dark place. Do not expose the module to sunlight or fluorescent light. Keep the temperature between 5˚C and 30˚C at humidity 50+-10%RH.

(b) The polarizer surface should not come in contact with any other object.

(c) It is recommended that they be stored in the container in which they were shipped.

(d) Storage condition is guaranteed under packing conditions.

(e) The phase transition of Liquid Crystal in the condition of the low or high storage temperature will be recovered when the LCD module returns to the normal condition

(2) High temperature or humidity may reduce the performance of module. Please store LCD module within the specified storage conditions.

(3) It is dangerous that moisture come into or contacted the LCD module, because the moisture may damage LCD module when it is operating.

(4) It may reduce the display quality if the ambient temperature is lower than 10 ºC. For example, the respons time will become slowly, and the starting voltage of lamp will be higher than the room temperature.

11.3 OTHER PRECAUTIONS

(1) Normal operating condition

(a) Display pattern: dynamic pattern (Real display)

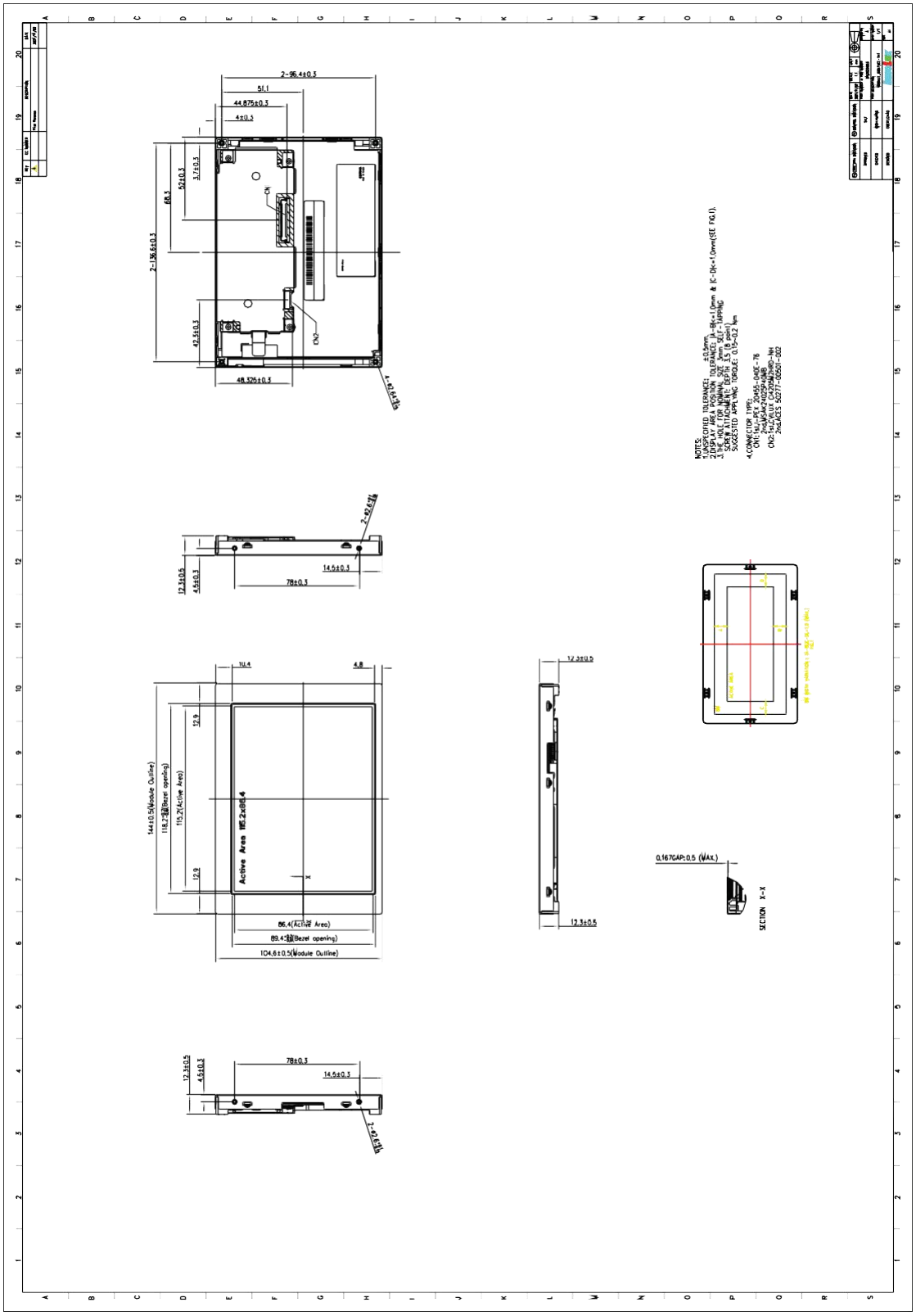
(Note) Long-term static display can cause image sticking.

(2) Operating usages to protect against image sticking due to long-term static display

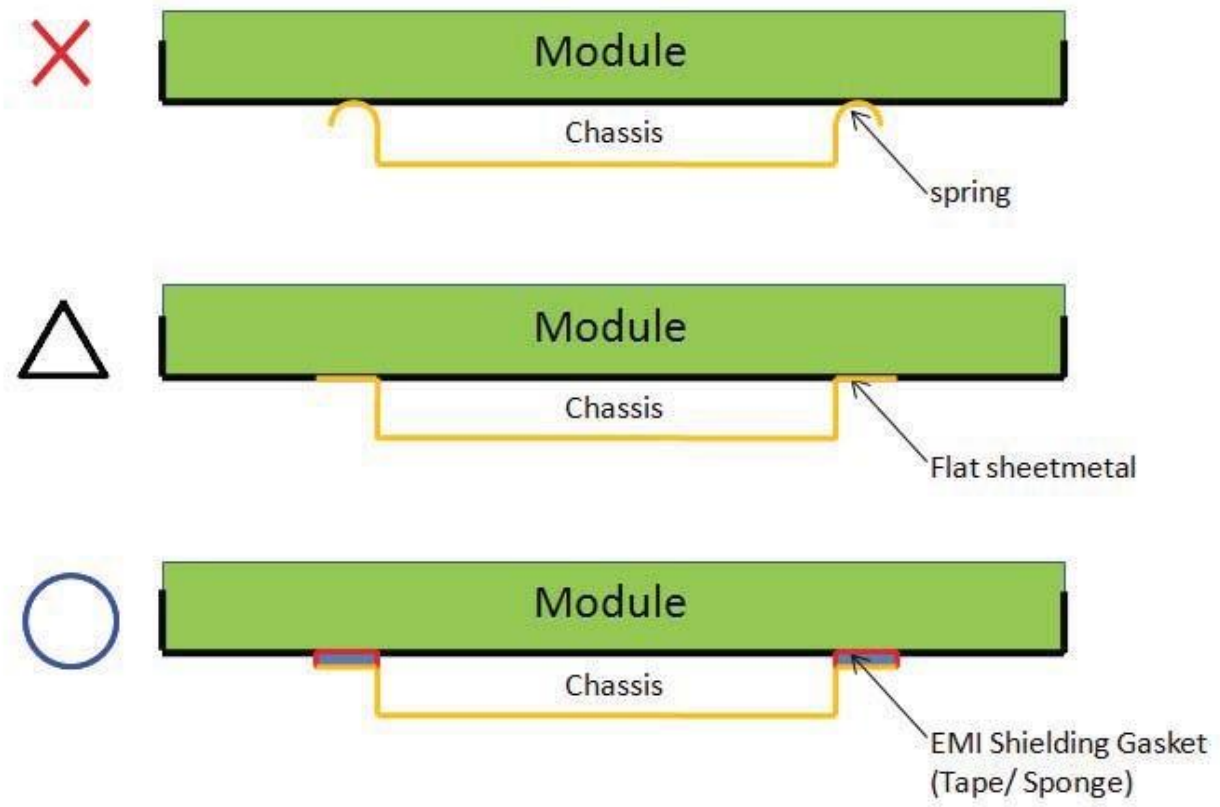
(a) Static information display recommended to use with moving image.

(3) Abnormal condition just means conditions except normal condition.

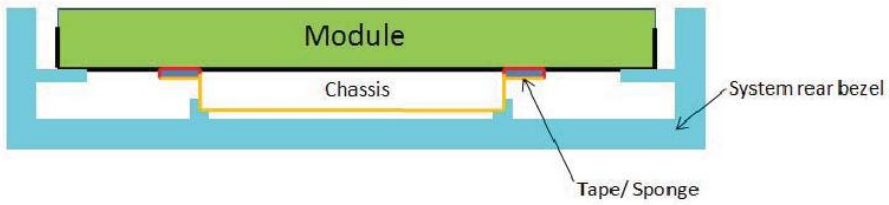
12. MECHANICAL CHARACTERISTICS

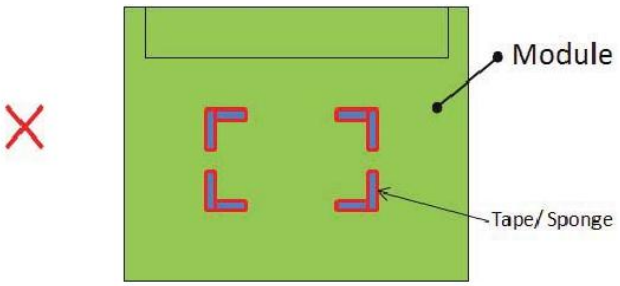


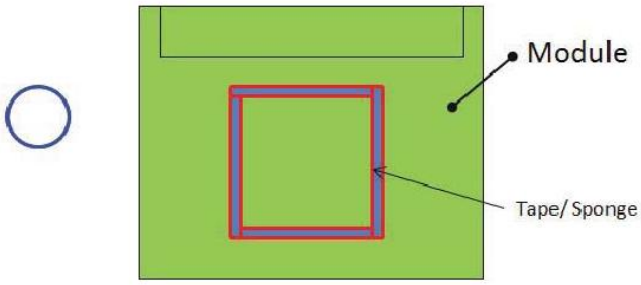
Appendix. SYSTEM COVER DESIGN NOTICE

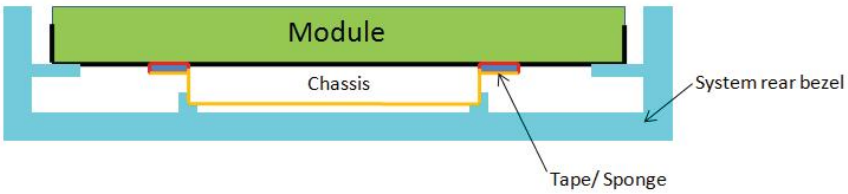
	Set Chassis and IAVM Module touching Mode
	
Definition	a. To prevent from abnormal display & white spot after mechanical test, it is not recommended to use spring type chassis. b. We suggest the contact mode between Chassis and Module rear cover is Tape/Sponge, second is Flat sheet metal type chassis.

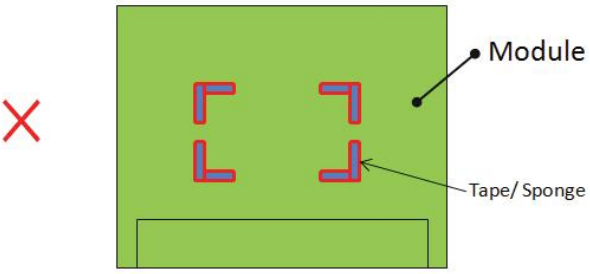
2	Tape/Sponge design on system inner surface

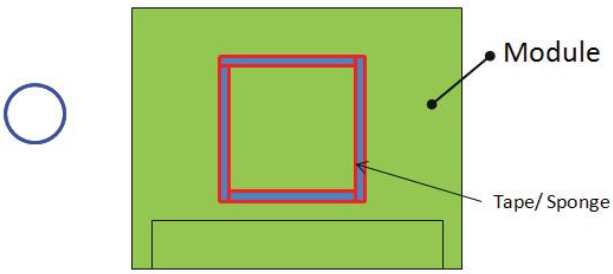




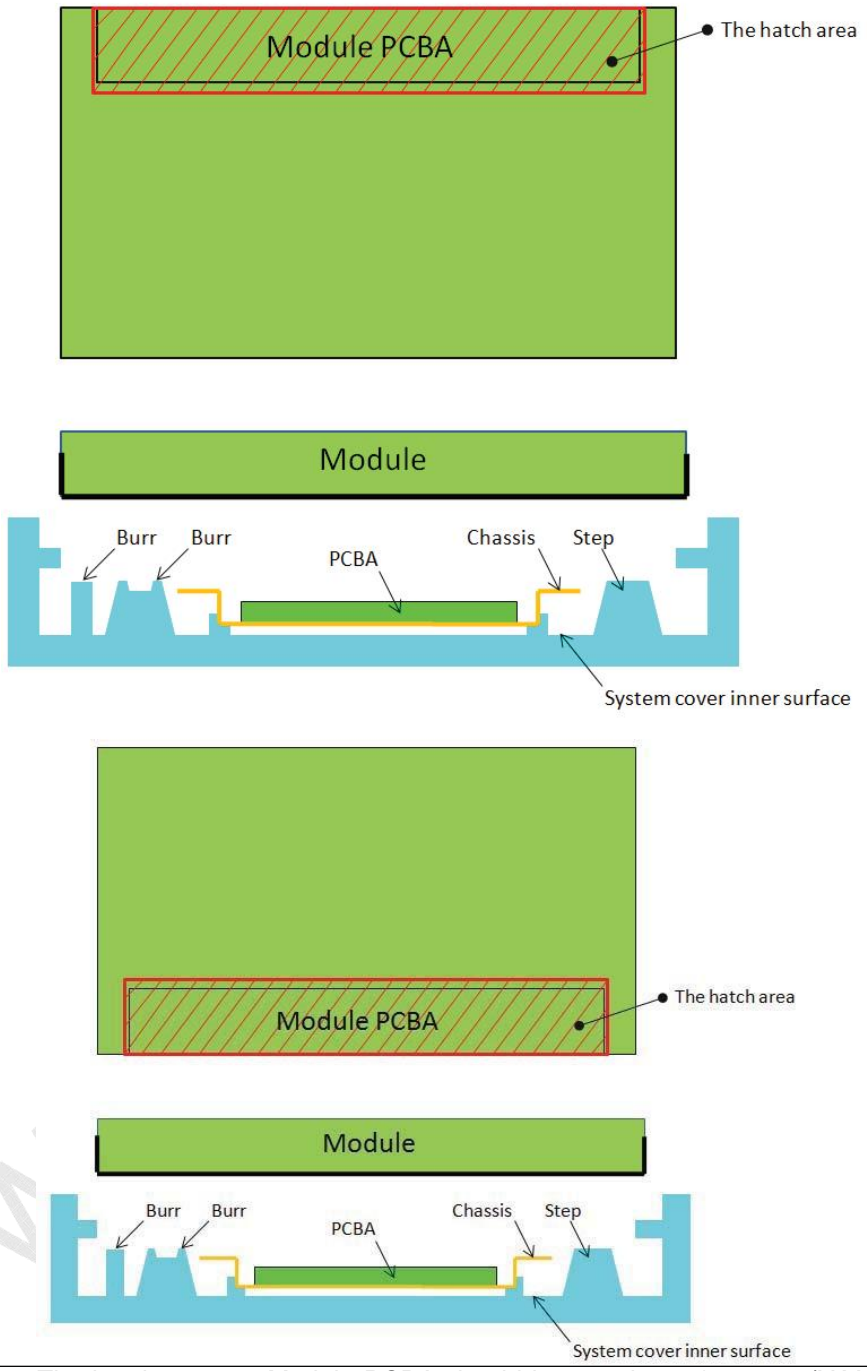


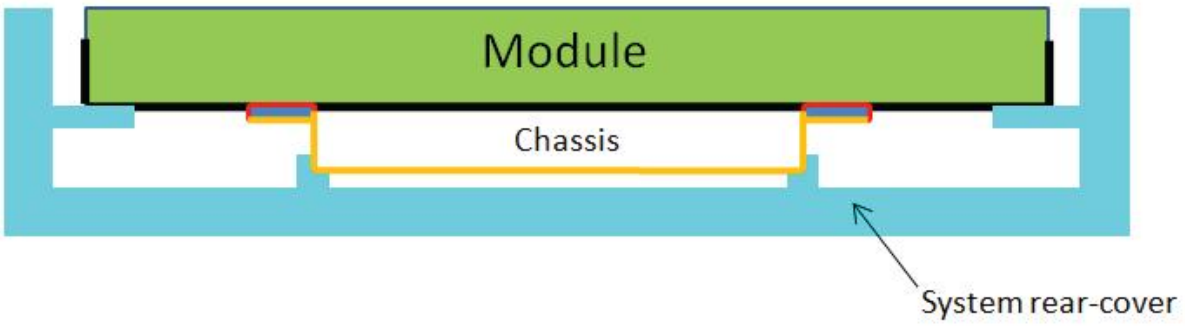


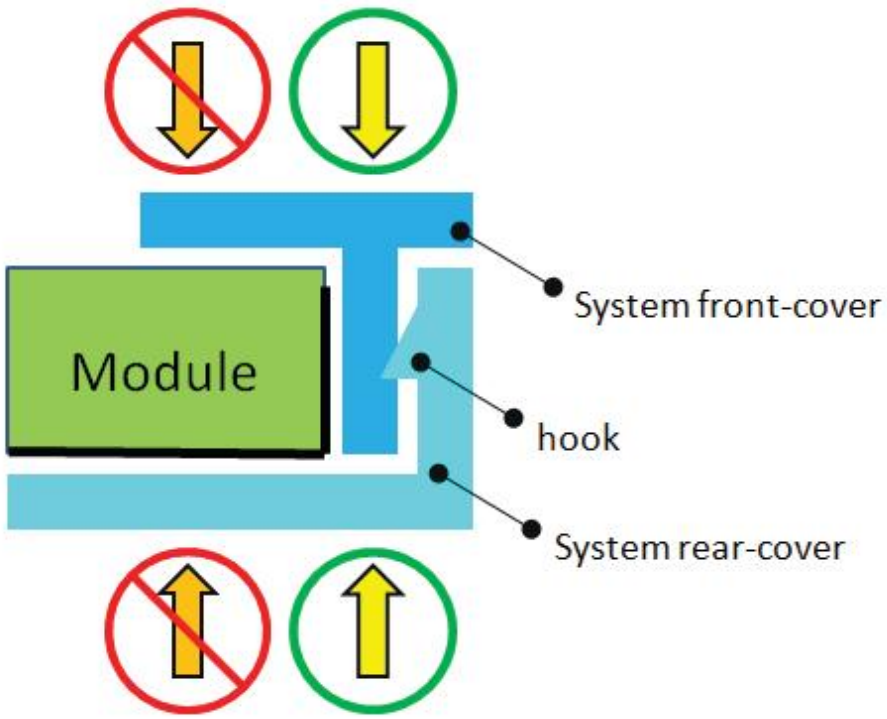


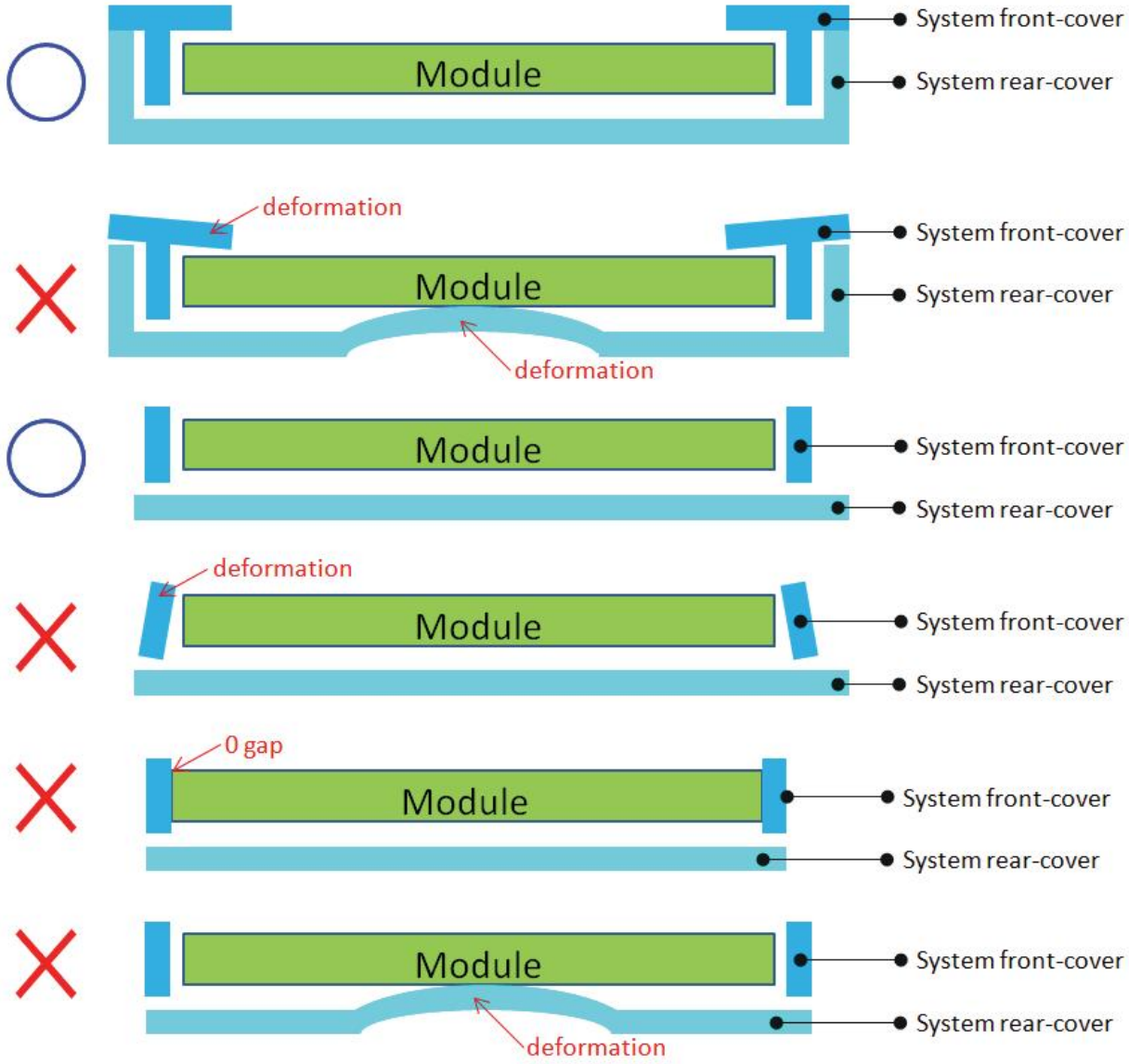


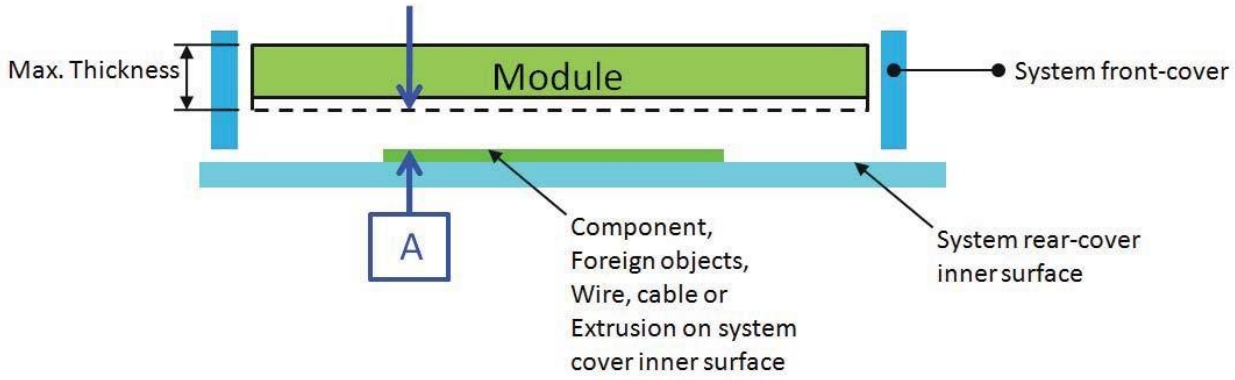
Definition	a. To prevent from abnormal display & white spot after mechanical test, we suggest using Tape/Sponge as medium between chassis and Module rear cover could reduce the occurrence of white spot. b. When using the Tape/Sponge, we suggest it be lay over between set chassis and Module rear cover. It is not recommended to add Tape/Sponge in separate location. Since each Tape/Sponge may act as pressure concentration location.

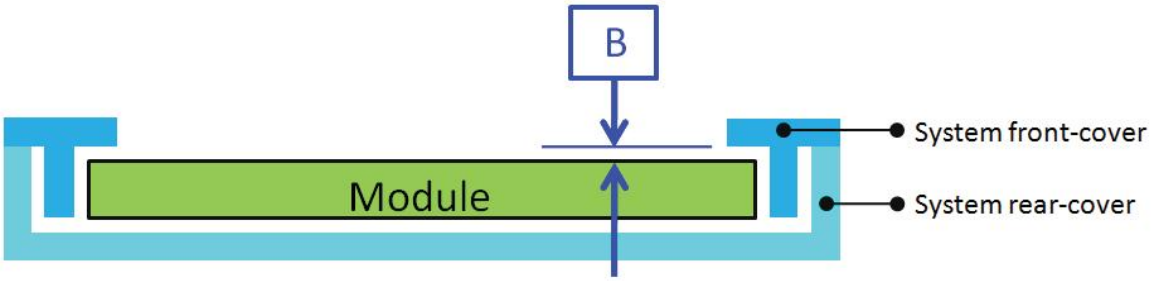
3	System inner surface examination
	
Definition	a. The hatch area on Module PCBA should keep at least 1mm gap(X,Y,Z direction) to any structure with system cover inner surface. b. Burr, Step, PCB protrusion may cause stress concentration. White spot may occur during reliability test.

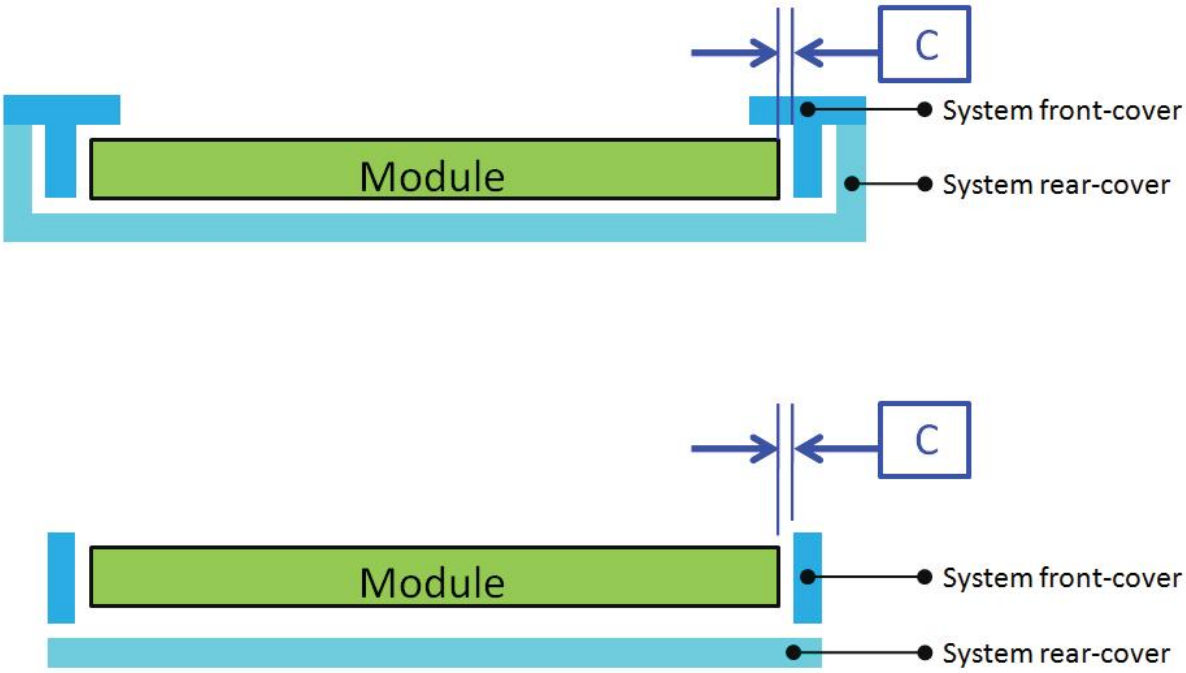
4	Material used for system rear-cover
	
Definition	System rear-cover material with high rigidity is needed to resist deformation during scuffing test, hinge test, pogo test or backpack test. Abnormal display, white spot, pooling issue may occur if low rigidity material is used. Pooling issue may occur because screw's boss position for module's bracket are deformed open-close test. Solid structure design of system rear-cover may also influence the rigidity of system rear-cover. The deformation of system rear-cover should not caused interference.

5	Assembly SOP examination for system front-cover with hook structure
	
Definition	To prevent panel crack during system front-cover assembly process with hook structure, it is not recommended to press panel or any location that relate directly to the panel.

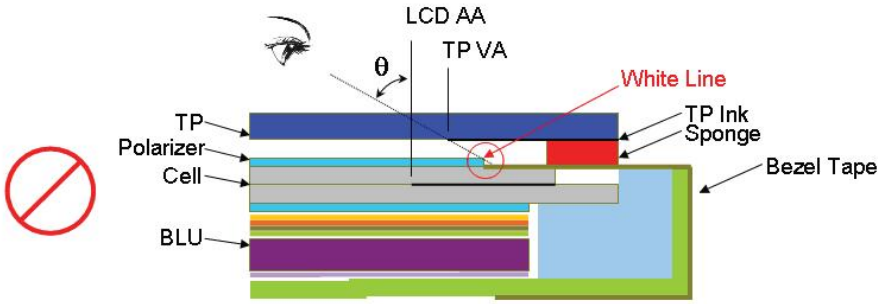
6	Permanent deformation of system cover after reliability test
	
Definition	System cover including front cover and rear cover may deform during reliability test. Permanent deformation of system front cover and rear cover after reliability test should not interfere with panel. Because it may cause issue such as pooling, abnormal display, white spot and also cell creak. Note: If the interference cannot be avoided, please feel free to contract INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.

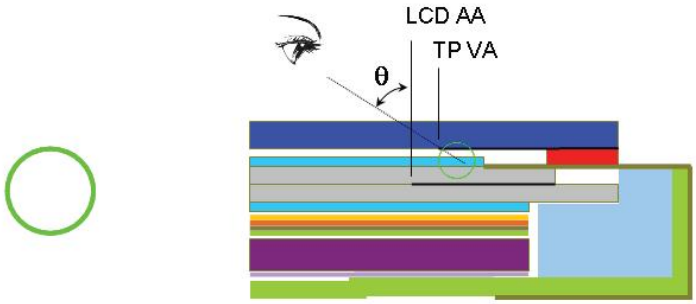
7	Design gap A between panel & any components on system rear-cover
	
Definition	System cover including front cover and rear cover may deform during reliability test. Permanent deformation of system front cover and rear cover after reliability test should not interfere with panel. Because it may cause issue such as pooling, abnormal display, white spot and also cell creak. Note: If the interference cannot be avoided, please feel free to contract INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.

8	Design gap B between system front-cover & panel surface
	
Definition	Gap between system front-cover & panel surface is needed to prevent pooling or glass broken. Zero gap or interference such as burr and warpage from mold frame may cause pooling issue near system front-cover opening edge. This phenomenon is obvious during swing test, hinge test, knock test or during pooling inspection procedure. To remain sufficient gap, design with system rib higher than maximum panel thickness is recommended. Note: If the interference cannot be avoided, please feel free to contract INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.

9	Design gap C between panel & system front-cover or protrusions
	
Definition	Gap between panel & system front-cover or protrusions is needed to prevent shock test failure. Because system front-cover or protrusions with small gap may hit panel during the test. Issue such as cell crack, abnormal display may occur. The gap should be large enough to absorb the maximum displacement during the test. Note: If the interference cannot be avoided, please feel free to contract INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.

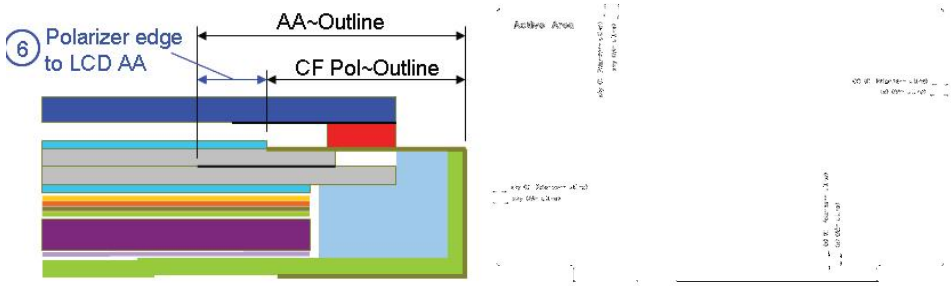
10	Touch Application : TP and LCD Module Combination for White Line Prevention



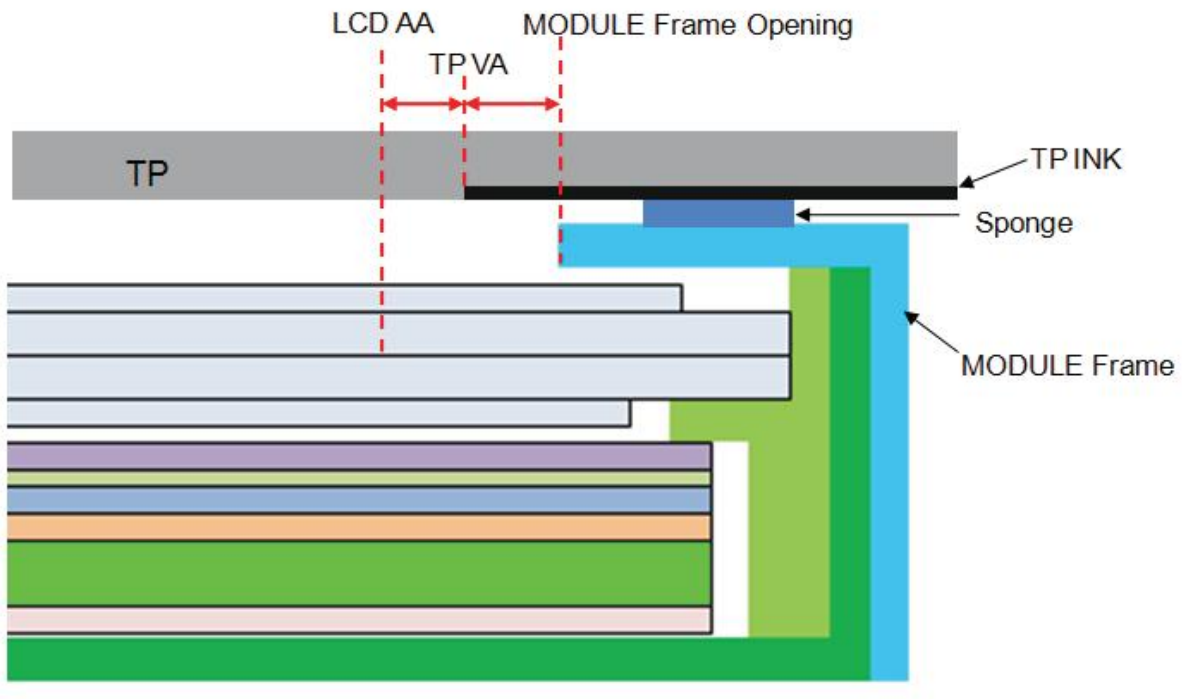


Parameter consideration for White Line Issue :	
1	TP VA to LCD AA distance
2	TP Assembly tolerance
3	TP Ink Printing tolerance
4	Sponge thickness and tolerance
5	Inspection/Viewing Angle specification
6	Polarizer edge to LCD AA distance and tolerance

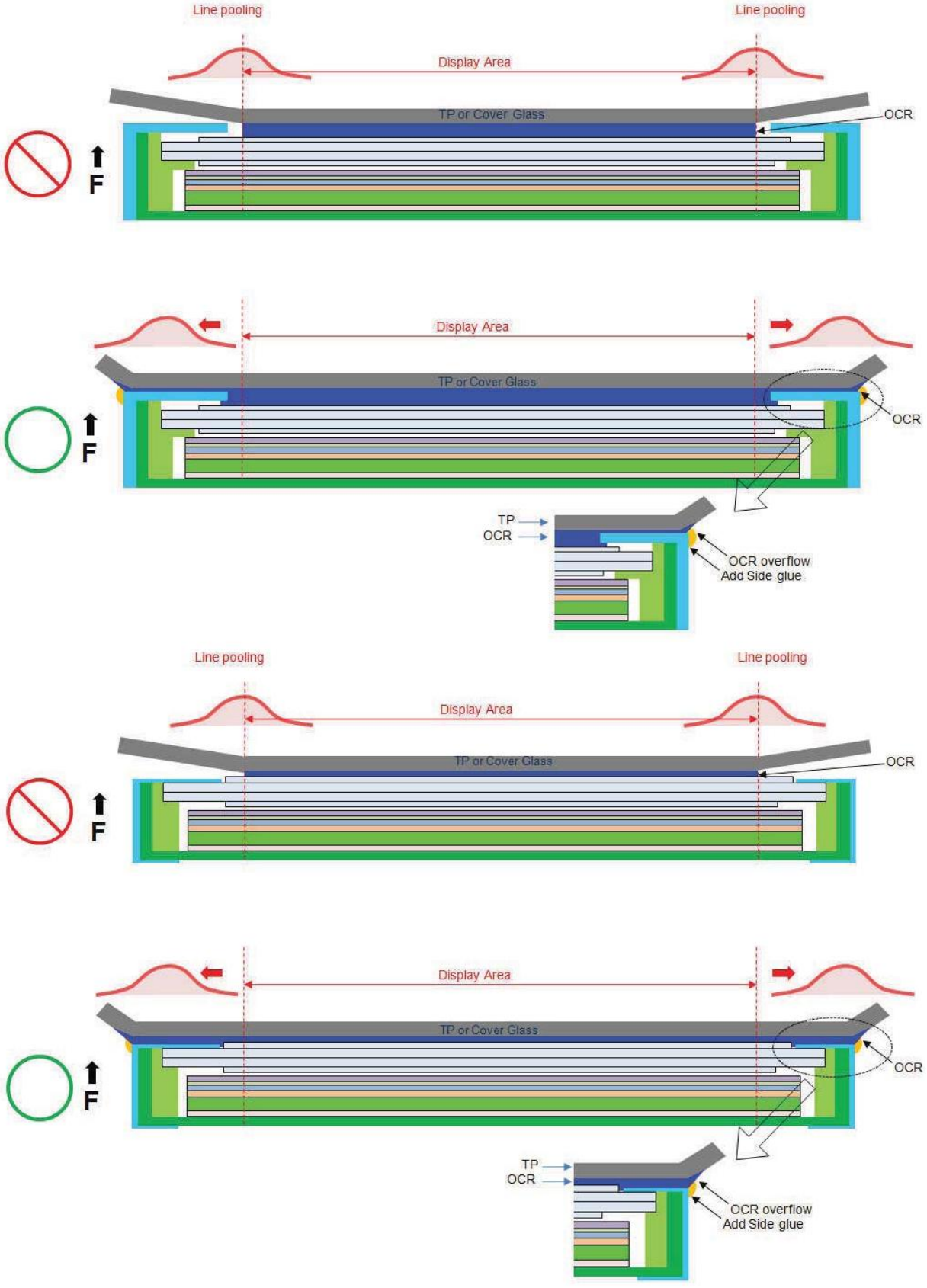
Polarizer edge to LCD AA distance can be derived by “AA~Outline” – “CF Pol~Outline” with respect to INX 2D Outline Drawing on each side.



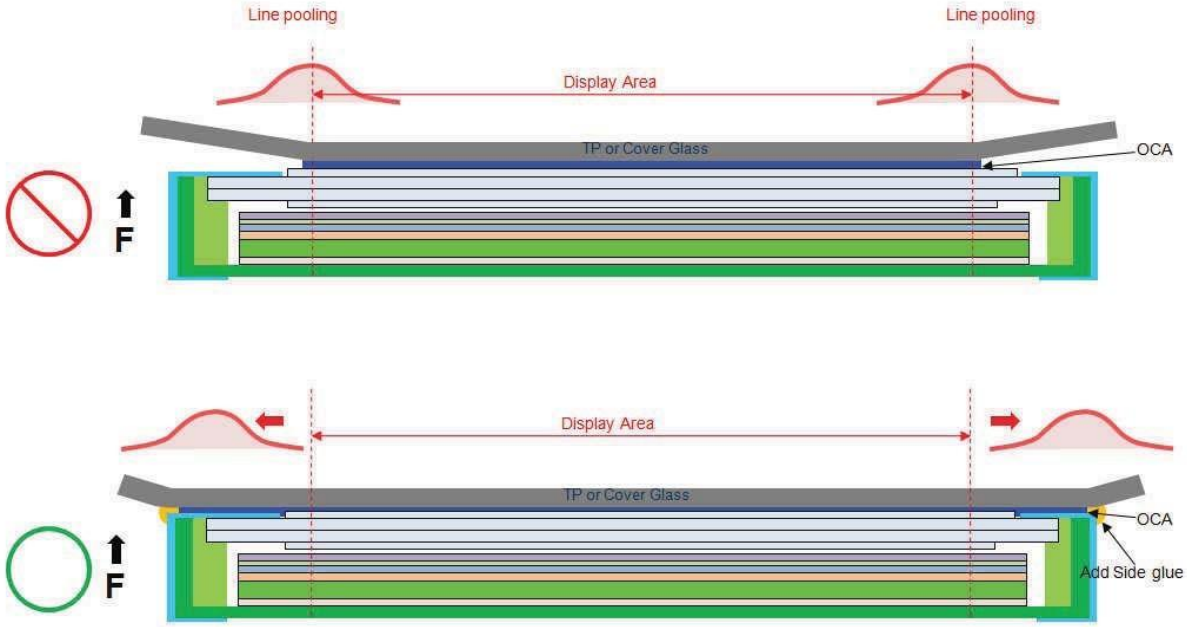
Definition	For using in Touch Application: to prevent White Line appears between TP and LCD module combination, the maximum inspection angle location must not fall onto LCD polarizer edge, otherwise light line near edge of polarizer will be appear. Parameters such as TP VA to LCD AA distance, TP assembly tolerance, TP Ink printing tolerance, Sponge thickness and tolerance, and Maximum Inspection/Viewing Angle, must be considered with respect to LCD module’s Polarizer edge location and tolerance. This consideration must be taken at all four edges separately. The goal is to find parameters combination that allow maximum inspection angle falls inside polarizer black margin area. Note: Information for Polarizer edge location and its tolerance can be derived from INX 2D Outline Drawing (“AA ~Outline“ - “CF Pol~Outline”). Note: Please feel free to contact INX FAE Engineer. By providing value of parameters above on each side, we can help to verify and pass the white line risk assessment for customer reference.

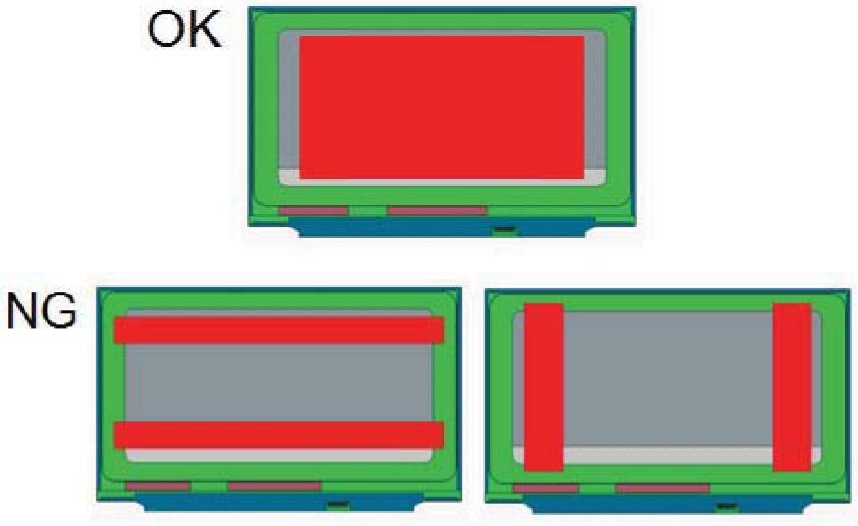
11	Design distance between TP AA to LCD AA
	
Definition	TP VA should avoid TP ink area covering LCD AA or causing the module frame to be exposed.

12	Use OCR Lamination

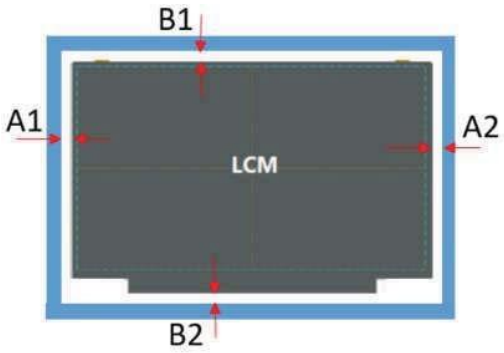


Definition	1. OCR glue as possible beyond module, in order to avoid Line Pooling 2. Add side glue to avoid Line Pooling

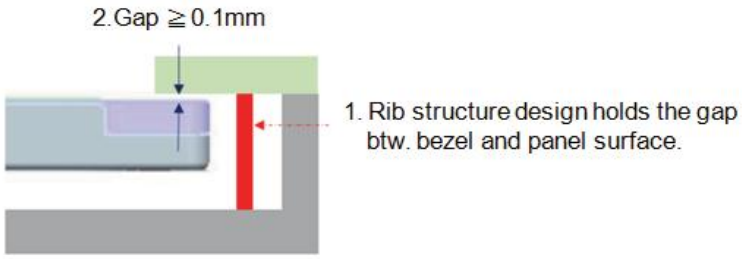
13	Use OCA Lamination
	
Definition	1. OCA glue as possible plastered throughout the module, in order to avoid Line Pooling. 2. Add side glue to avoid Line Pooling

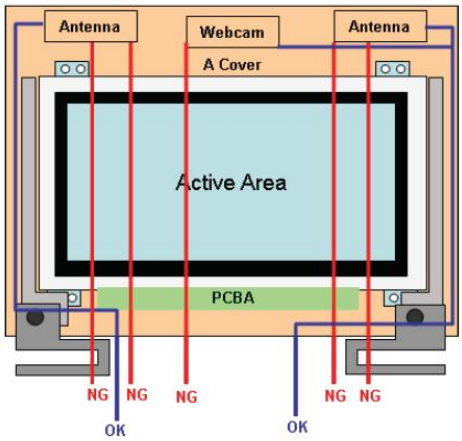
1	Sponge area design behind panel
	
Definition	Sponge area design behind panel can not be across the panel metal rear and the reflector at the same time. It can be on the reflector area only.

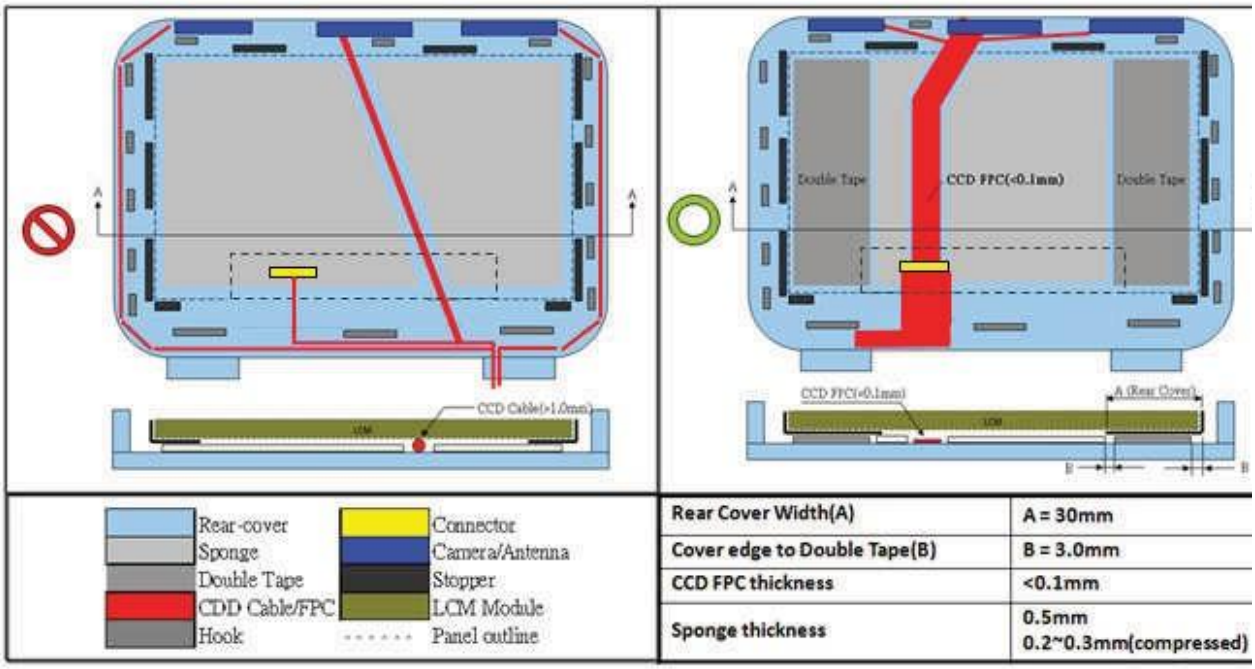
2	Gap between system rear-cover & panel
	
Definition	The maximum thickness of sponge on the system rear-cover can not interfere to the maximum thickness of panel. Because the interference may cause stress concentration. Issues such as pooling, abnormal display, white spot, and cell crack may occur. Note: If the interference can not be avoided, please feel free to contact INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.

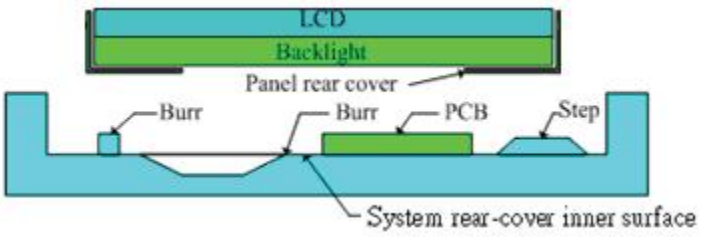
3	Gap Design between panel & around structure
	
Definition	Gap Design between panel & around structure needs to consider the maximum tolerances of panel outline and assembly at the same time. Gap Design suggestion is shown as A1/A2/B1/B2 on the chart.

Item	Suggestion	Remark
A1	A1≧0.5	Gap≧ Panel outline max. tolerance + Assembly max. tolerance
A2	A2≧0.5	
B1	B1≧0.5	
B2	B2≧0.8	

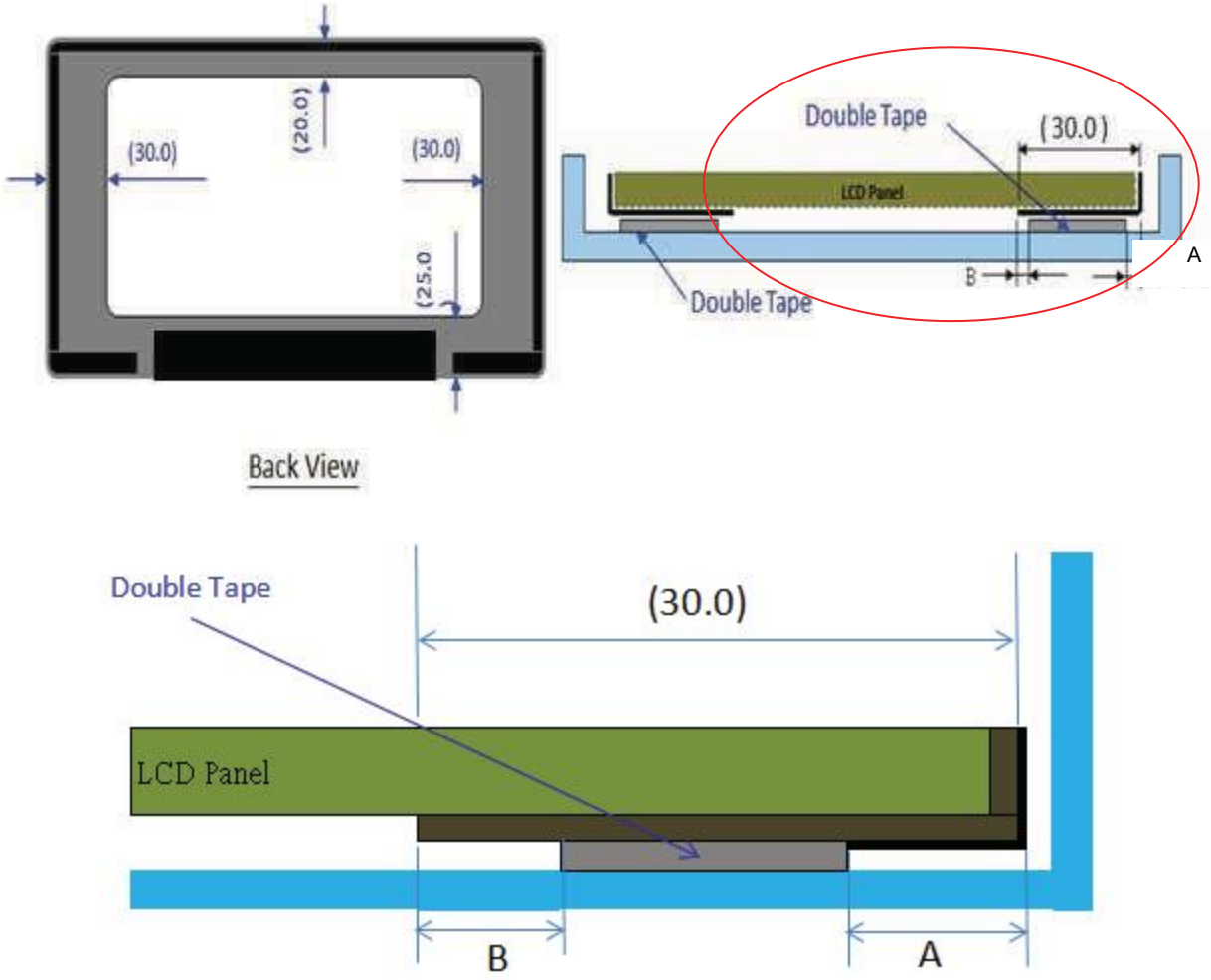
4	Gap between panel & bezel
	
Definition	The gap between system bezel & panel surface is needed to prevent pooling or glass broken. Zero gap or interference such as burr and warpage from mold frame may cause pooling issue near system font-cover opening edge. This phenomenon is obvious during swing test, hinge test, knock test, or during pooling inspection procedure. To remain the sufficient gap, design with system rib higher than maximum panel thickness is recommended. The sufficient gap design is greater or equal to 0.1mm.

5	Cable routing behind panel
	
Definition	It is strongly recommended that cables route around the panel outline, not overlap with the panel outline (including PCB). Because issue such as abnormal display & white spot after backpack test, hinge test, twist test or pogo test may occur. If any routings across panel outline are needed, we suggest design as below: -Using FFC/FPC to replace cables. -Routing at the right or left area of panel metal rear. -Avoid any routings at the step of panel or A cover. -No interference to panel. -It should not overlap TCON, COF/FPC, Driver IC

6	Interference examination of antenna cable and Web Cam wire
	• To prevent panel damage, we suggest using CCD FPC to replace CCD cable • Using double tape to fix LCM module for no bracket design.  Rear Cover Width(A): A = 30mm Cover edge to Double Tape(B): B = 3.0mm CCD FPC thickness: <0.1mm Sponge thickness: 0.5mm / 0.2~0.3mm(compressed)
Definition	If the antenna cable or Web Cam wire must overlap with the panel outline, both sides of the antenna cable or Web Cam wire must have a sponge(Sponge material can not contain NH3) and sponge require higher antenna cable or Web Cam wire.(Antenna cable or Web Cam wire should not overlap with TCON,COF/FPC,Driver IC) Note: If the interference can not be avoided, please feel free to contact INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.

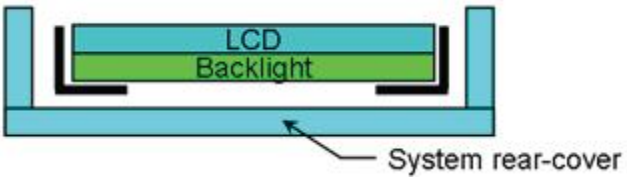
7	System rear-cover inner surface examination
	
Definition	Burr at logo edge, steps, protrusions or PCB board may cause stress concentration. White spot or glass broken issue may occur during reliability test.

8	Tape/sponge design on system inner surface



Definition	To prevent peeling the bezel tape in rework process. The length of double tape is 30 – (A+B), A is bezel tape length and B is the double tape attaching tolerance. Ex :A :2mm, B:2mm, the length of double tape is 30-(2+2)=26mm.

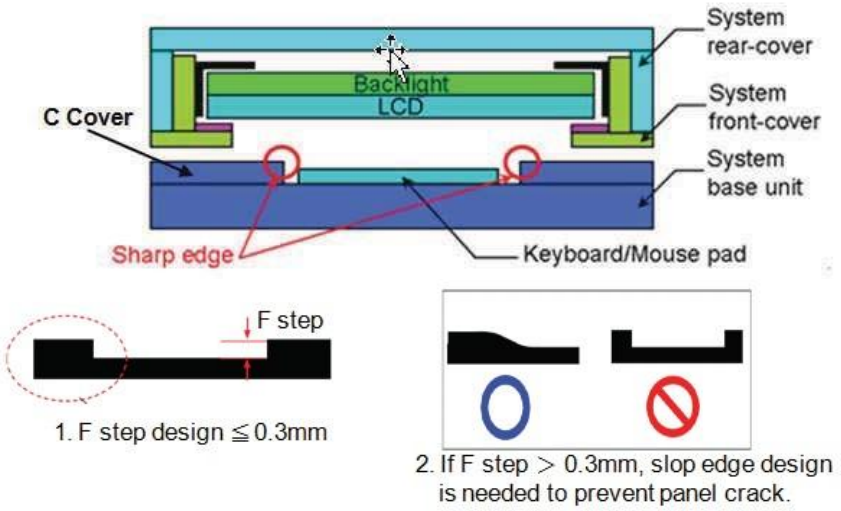
9	Material used for system rear-cover

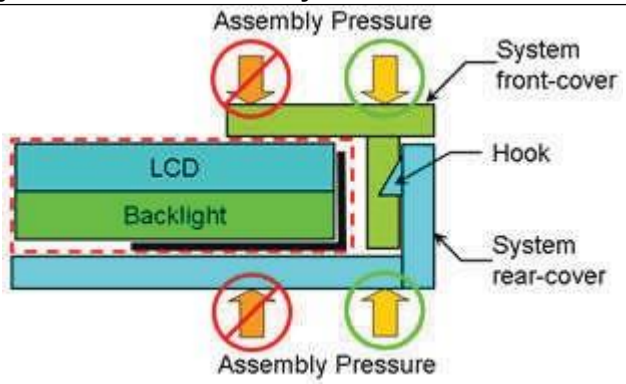


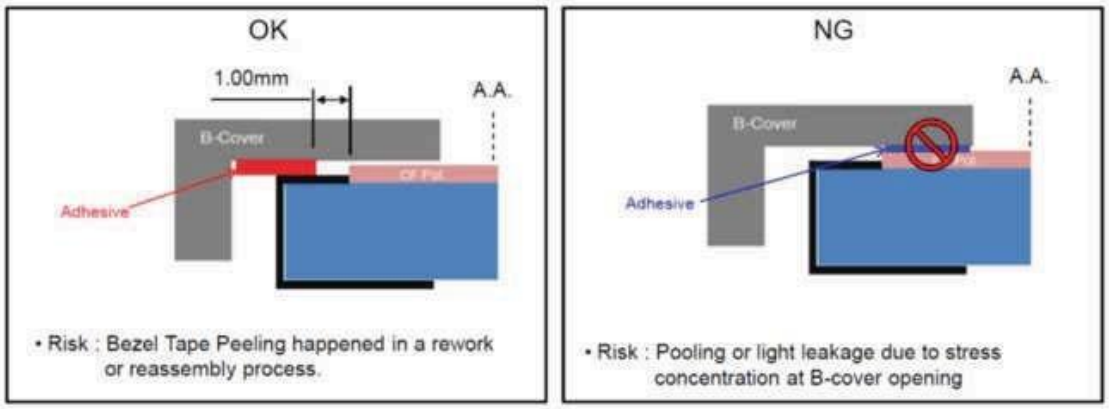
System rear-cover material: Al-Mg alloy

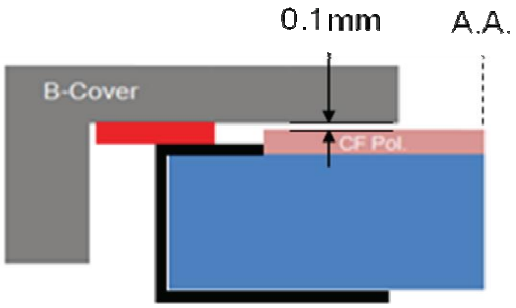
System rear-cover thickness:1.5mm

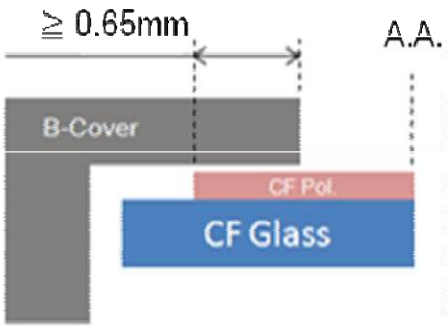
Definition	System rear-cover material with high rigidity is needed to resist deformation during scuffing test, hinge test, pogo test, or backpack test. Abnormal display, white spot, pooling issue may occur if low rigidity material is used. Solid structure design of system rear-cover may also influence the rigidity of system rear-cover. The deformation of system rear-cover should not caused interference.

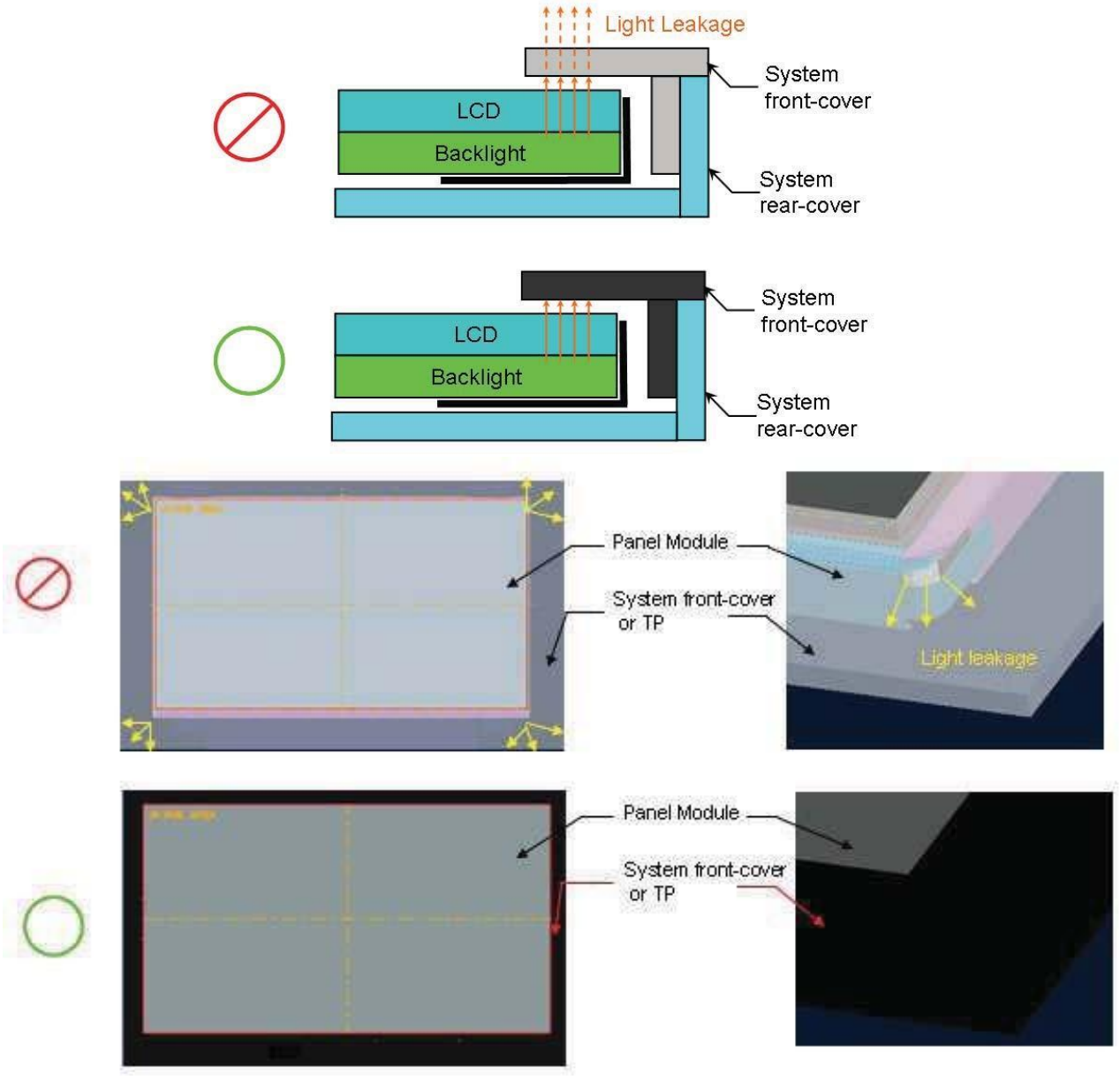
10	C cover shape design
	
Definition	The F step design on C Cover less than or equal to 0.3mm is recommended. If F step exceeds 0.3mm, the slop edge design is necessary to prevent panel crack.

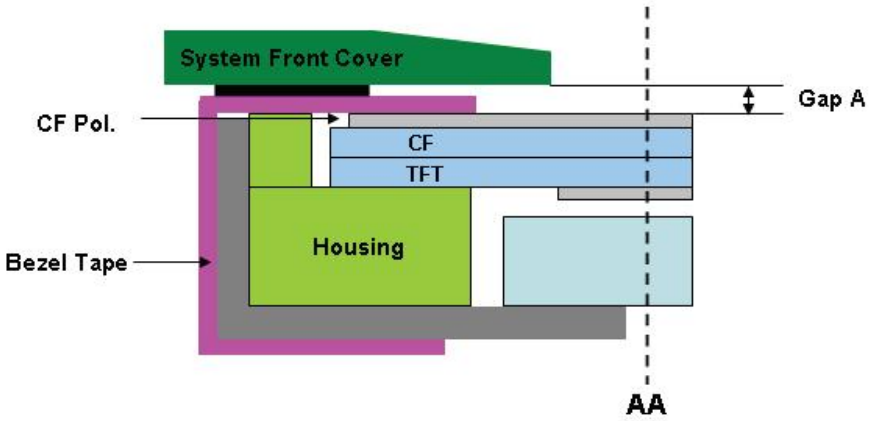
11	Assembly SOP examination for system front-cover with Hook design
	
Definition	To prevent panel crack during system front-cover assembly process with hook design, it is not recommended to press panel or any location that related directly to the panel.

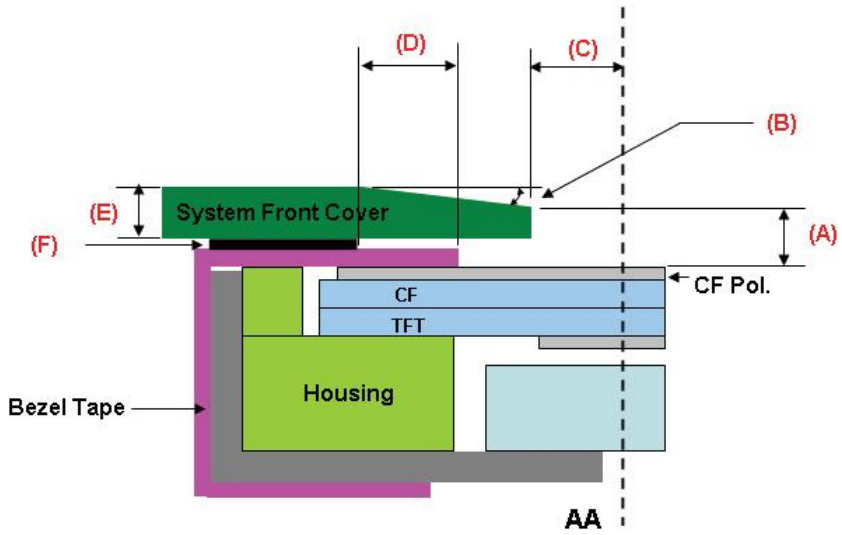
12	Adhesive design between panel & bezel
	
Definition	To prevent panel crack during system front-cover assembly process with double tape design, When system applied adhesive between B-Cover and LCD module, please design a distance 1.00mm between B-Cover's adhesive and CF pol. Do **NOT** put adhesive on CF pol. Adhesive material need be qualified to prevent from doing damage to cell tape after rework. Adhesive material need be qualified to prevent abnormal noise when hinge swinging test.

13	System front-cover assembly reference with Double tape design
	
Definition	To prevent system front-cover peeling at double tape contact area, A gap between B-Cover & CF-Pol. Is 0.1mm min.

14	System front-cover opening area reference with TFT-LCD module
	
Definition	To prevent panel the noise of B-cover & CF Pol. Distance from CF Pol. edge to front-cover edge more than 0.65mm.

15	Color of system front-cover material
	
Definition	To prevent light leakage is seen at system front-cover due to material transparency, we suggest using dark color material (black) for system front-cover design.

16	Design Gap between System Front-cover & TOD LCD module surface
	 **0.15 ≤ Gap A ≤ 0.20 mm**
Definition	Gap A between system front-cover & TOD LCD module surface is needed to prevent pooling or glass broken. Zero gap or interference such as burr and warpage from mold frame may cause pooling issue near system font-cover opening edge. This phenomenon is obvious during swing test, hinge test, knock test, or during pooling inspection procedure. To remain sufficient gap for first graph, design value for front-cover depth is recommended higher than module wing depth.

17	System Front-cover dimension suggestion
	

System Front Cover Open TOP to CF Pol. (A)	System Front Cover Chamfer (B)	System Front Cover Open to AA (C)	Bezel Tape Edge to Double Tape (D)	System Front Cover thickness (E)	Double Tape Thickness (F)
0.8mm Max	8~20°	0.7≦ (B) ≦ 0.9mm	1.0 mm Min	1.2mm MAX	0.05≦ (F) ≦ 0.08mm

CAUTION :
In order to avoid the risk of bezel tape peeling, INX suggest not to attach any double tape on bezel tape; if necessary, the location of duuble tape attach must follow INX design guidance.

Definition	To achieve better touch sensibility, INX suggests to follow design value as recommended , Recommended dimension is shown in above graph.